

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau(43) International Publication Date
3 January 2003 (03.01.2003)

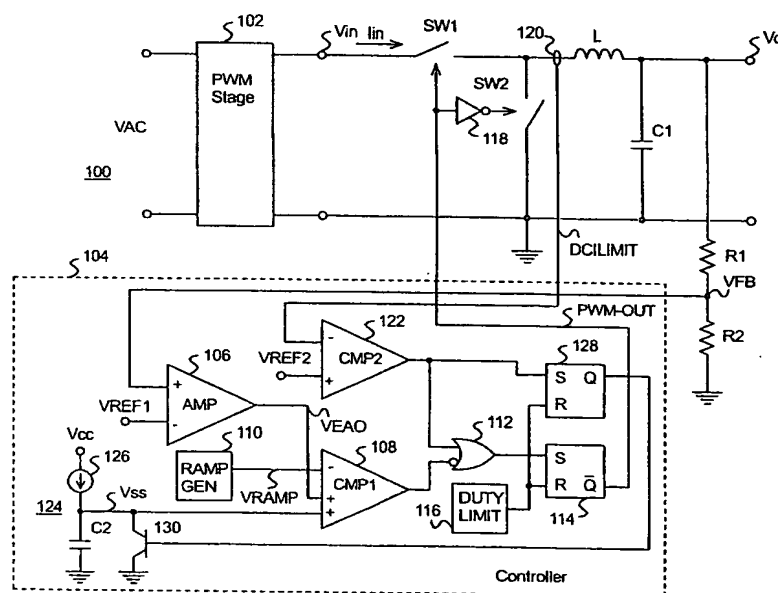
PCT

(10) International Publication Number
WO 03/001314 A1

- (51) International Patent Classification⁷: G05F 1/46, 1/56, 1/565, 1/573
- (21) International Application Number: PCT/US02/19890
- (22) International Filing Date: 21 June 2002 (21.06.2002)
- (25) Filing Language: English
- (26) Publication Language: English
- (30) Priority Data: 60/300,492 21 June 2001 (21.06.2001) US
- (71) Applicant (for all designated States except US): CHAMPION MICROELECTRONIC CORP. [US/US]; 4020 Moorpark Avenue, Suite 105, San Jose, CA 95117 (US).
- (72) Inventor; and
- (75) Inventor/Applicant (for US only): HWANG, Jeffrey [US/US]; 20576 Manor Drive, Saratoga, CA 95070 (US).
- (74) Agents: WESTBERG, Derek, J.; Stevens & Westberg, LLP, 99 North First Street, Suite 201, San Jose, CA 95113 et al. (US).
- (81) Designated States (national): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, OM, PH, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VN, YU, ZA, ZM, ZW.
- (84) Designated States (regional): ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).
- Published: — with international search report

[Continued on next page]

(54) Title: CURRENT LIMITING TECHNIQUE FOR A SWITCHING POWER CONVERTER



(57) Abstract: An improved technique for limiting current in a switching power converter (100). The switching power converter includes a soft-start circuit (104) which slowly increases a switching duty cycle upon power-up. Once the converter is operating normally, the duty cycle is controlled to regulate the output voltage. In the event an excessive output current is detected, soft-start circuit is controlled to reduce the switching duty cycle. More particularly, a soft-start capacitor may be discharged during portions of a clock period used to control switching.



For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

CURRENT LIMITING TECHNIQUE FOR A SWITCHING POWER CONVERTER

This application claims the benefit of U.S. Provisional Application Serial No.
5 60/300,492, filed June 21, 2001.

Field of the Invention:

The invention relates to switching power converters. More particularly, the
invention relates to a technique for limiting current by limiting a switching duty cycle in
10 such a power converter.

Background of the Invention:

In a conventional switching power converter, provision may be made for limiting
current to a load in the event the load experiences a fault. For example, U.S. Patent No.
15 5,742,151 discloses a PFC-PWM power converter in which the output current developed
by the PWM section is limited in when an excessive output current is detected. More
particularly, for each switch cycle, the switch is closed upon sensing an excessive output
current. A drawback to this technique is that when the switch is opened for each
switching cycle, an excessive current can occur before the switch is closed in response to
20 the excessive current. This repeated occurrence of excessive current may cause excessive
power dissipation in the converter.

What is needed is an improved current limiting technique for a switching power
converter. It is to these ends that the present invention is directed.

25 Summary of the Invention:

The present invention is an improved technique for limiting current in a switching
power converter. The power converter includes a switch for transferring energy from a
source to the load by opening and closing the switch according to a duty cycle. A duty
cycle limiter is triggered when the output current of the converter exceeds a
30 predetermined level. The duty cycle is limited to an amount that is related to a degree to
which the output current is excessive. In one aspect, the duty cycle limiter include a

capacitor having a charge that is gradually changed in response to the output current exceeding the predetermined level where the duty cycle is related to a voltage on the capacitor. In another aspect, the duty cycle limiter includes a counter where the duty cycle is related to a count of the counter. In another aspect, the duty cycle limiter
5 provides a soft-start in which the switching duty cycle is gradually increased upon power-up. Once the converter is operating normally, the duty cycle is controlled to regulate the output voltage.

The invention has an advantage in that by reducing the switching duty cycle, the output current is reduced and is, thus, less likely to reach an excessive level upon each
10 cycle of the switch. In comparisons to prior techniques, this reduces power dissipation in the converter.

Brief Description of the Drawings:

Figure 1 illustrates a schematic diagram of a power converter in accordance with
15 an aspect of the present invention;

Figure 2 illustrates a schematic diagram of an alternate embodiment of a power converter in accordance with an aspect of the present invention;

Figures 3a and 3b illustrate a schematic diagram of a two-stage power factor correction and pulse width modulation power converter in accordance with an aspect of
20 the present invention;

Figure 4 illustrates an exemplary three-input comparator that may be used with the power converters of the present invention; and

Figures 5a and 5b illustrate a schematic diagram of a two-stage power factor correction and pulse width modulation power converter in accordance with an aspect of
25 the present invention.

Detailed Description of a Preferred Embodiment:

Figure 1 illustrates a schematic diagram of a power converter 100 in accordance with an aspect of the present invention. An input voltage V_{in} may be applied to a first
30 terminal of a main power switch SW1 (e.g., a transistor switch). A second terminal of the switch SW1 may be coupled to a first terminal of a second switch SW2 (e.g., a transistor

switch) and to a first terminal of an inductor L. A second terminal of the inductor L may be coupled to a first terminal of a capacitor C1. A second terminal of the switch SW2 and a second terminal of the capacitor C1 may be coupled to a ground node. It will be apparent that the switch SW2 may be replaced by a diode.

5 A source 102 of the input voltage V_{in} may include a power factor correction (PFC) stage of the power converter 100. Thus, the source 102 may receive an alternating current (AC) signal and perform power factor correction in which current drawn from AC source VAC is maintained substantially in phase with the AC voltage signal so as to present a resistive load to the AC source. It will be apparent, however, that the PFC stage
10 may be omitted, in which case, the input voltage V_{in} may be provided by another source that provides a regulated voltage, an unregulated voltage or a loosely-regulated voltage.

 When the switch SW1 is closed, the switch SW2 is open. Under these conditions, current I_{in} from the source 102 charges the inductor L with energy. When the switch SW1 is opened, the switch SW2 is closed. Under these conditions, energy from the
15 inductor L charges the capacitor C1 with energy. An output voltage V_o formed across the capacitor C1 may be used to power a load (not shown). The level of power delivered to the load may be adjusted according to the duty cycle of the switches SW1 and SW2.

 A controller 104 may control the duty cycle of the switches SW1 and SW2 so as to maintain the output voltage V_o at a desired level. For this purpose, a first terminal of a
20 resistor R1 may be coupled to receive the output voltage V_o . A second terminal of the resistor R1 may be coupled to a first terminal of a resistor R2. A second terminal of the resistor R2 may be coupled to a ground node. Accordingly, the resistors R1 and R2 form a resistive divider in which a feedback signal VFB formed at an intermediate node of the resistive divider is representative of the level of the output voltage V_o .

25 The feedback signal VFB may be coupled to a first input terminal of an amplifier 106. Reference voltage V_{REF1} that is representative of a desired level for the output voltage V_o may be coupled to a second input of the amplifier 106. Accordingly, an output of the amplifier 106 forms an error signal VEO that is representative of a difference between the output voltage V_o and a desired level for the output voltage. The
30 error signal VEO may be coupled to a first input of a comparator 108. A second input

of the comparator 108 may be coupled to receive a periodic ramp signal VRAMP from a ramp generator 110.

The output of the comparator 108 forms a switch control signal VSC. When the level of the ramp signal VRAMP is below the level of the error signal VEO, the switch control signal VSC may be a logic high voltage. Then, as the ramp signal rises, it eventually exceeds the level of the error signal VEO. In response, the switch control signal VSC may transition to a logic low voltage until the ramp signal VRAMP is reset and the process repeats. Thus, the duty cycle of the switch control signal VSC is adjusted depending upon the level of the output voltage V_o .

The switch control signal VSC may be coupled to a first (inverting) input of a logic OR gate 112. An output of the logic gate 112 may be coupled to a set input S of a flip-flop or latch 114. A reset input R of the flip-flop 114 may be coupled to receive a periodic clock signal from a duty-cycle limiter 116. A \overline{Q} (inverted) output PWM-OUT of the flip-flop 114 may be coupled to control the switch SW1 and the switch SW2 (via an inverter 118).

When the flip-flop 114 is reset by the duty-cycle limiter 116, the switch SW1 is closed and the switch SW2 is opened. In addition, the ramp signal VRAMP, being synchronized with the periodic clock signal from the duty-cycle limiter 116, is reset to its initial value from which it begins to rise. Under these conditions, the switch control signal VSC is a logic high voltage and the output of the logic gate 112 is a logic low voltage. Then, when the level of the ramp signal VRAMP exceeds the level of the error signal VEO, the switch control signal VSC transitions to a logic low voltage. As a result, the flip-flop 114 is set and the switch SW1 is opened and the switch SW2 is closed. The switch SW1 remains open and the switch SW2 remains closed until the flip-flop 114 is once again reset by the duty-cycle limiter 116.

The signal PWM-OUT may differ from the signal VSC in that the signal PWM-OUT may be duty-cycle limited by a duty cycle limiter 116. The duty cycle limiter 116 may form a periodic square wave signal whose duty cycle is equivalent to a maximum duty cycle allowed for the switch SW1.

When the output voltage V_o rises, the error signal VEO also rises. As a result, the switch SW1 remains open for a longer portion of the switching cycle because more

time is required for the ramp signal VRAMP to exceed the error signal VEAO. Thus, the switching duty-cycle is reduced which tends to reduce the output voltage Vo.

Conversely, when the output voltage Vo falls, the error signal VEAO also falls. As a result, the switch SW1 remains open for a shorter portion of the switching cycle because less time is required for the ramp signal to exceed the error signal VEAO. Thus, the switching duty-cycle is increased which tends to increase the output voltage Vo.

Accordingly, the output voltage Vo is regulated in a closed feedback loop.

The power converter 100 of Figure 1 is exemplary. Thus, it will be apparent that modifications can be made. For example, the exemplary power converter 100 uses trailing-edge modulation, however, leading-edge modulation may be used. As another example, the power converter 100 has buck converter topology. However, another type of converter topology may be used, such as that of a boost converter.

A current sensor 120 may be coupled to sense current in the converter 100. As shown in Figure 1, the current sensor 120 may sense current in the inductor L.

Alternately, the current sensor 120 may sense current in the switch SW1 or the switch SW2. In either case, the current sensor 120 senses a current that is representative of an output current provided to the load. Further, the current sensor 120 may be implemented in a number of different ways. For example, a resistor that is configured to receive the current to be sensed forms a voltage that is representative of the current. As another example, a current may be induced in the secondary winding of a transformer or coupled inductor. Thus, current in the inductor L may be sensed via an induced current in a second inductor (not shown) that is inductively coupled to the inductor L. Further, the current sensor 120 may form a signal that is representative of an average of the sensed current, such as by use of a filter.

The current sensor 120 forms a voltage signal DCILIMIT that is representative of the sensed current. This current-sensing signal may be coupled to a first input of a comparator 122. A second input of the comparator 122 may be coupled to receive a reference voltage VREF2 that is representative of a maximum desired level for the sensed current. An output of the comparator 122 may be coupled to a second input of the logic OR gate 112. Thus, the output of the comparator 122 may open the switch SW1 in the event that a current sensing signal DCI LIMIT exceeds a predetermined level.

As explained above, under normal operating conditions, the comparator 108 compares a signal VFB that is representative of an output voltage V_o of the converter 100 to a periodic ramp signal VRAMP in order to adjust the duty cycle of the switch SW1. Accordingly, the output voltage V_o is regulated in a feedback loop.

5 Upon start-up, however, a duty cycle limiting circuit arrangement 124 may provide a soft-start in which the duty cycle of the switch SW1 is limited so as to prevent excessive current in the switch SW1. Thus, a soft-start voltage V_{ss} formed across a soft-start capacitor C2 is initially a low voltage level, when the output voltage V_o is significantly lower than the desired level. Over time, a current source 126 charges the
10 capacitor C2. Initially, when the signal V_{ss} is higher than the signal VEO, the voltage V_{ss} is compared by comparator 108 to the periodic ramp signal VRAMP. As the soft-start signal V_{ss} increases, so does the duty cycle of the switch SW1. As a result, the output voltage V_o increases. Once the level of VEO rises above the level of V_{ss} , then the comparator 108 compares the signal VFB to the ramp signal VRAMP to control the
15 duty cycle of the switch SW1. Accordingly, the comparator 108 compares the higher one of the two signals V_{ss} and VEO to the ramp signal VRAMP to control the duty cycle of the switch SW1.

The voltage signal DC ILIMIT is representative of the output current of a PWM stage of the converter 100 and is coupled to the comparator 122. In response to the signal
20 DC ILIMIT exceeding a predetermined level of the reference voltage VREF2 (e.g., 1.0 volt), the comparator 122 opens the switch SW1 via a logic OR gate 112. Optionally, the comparator 122 may be disconnected from the logic OR gate 112 and the logic OR gate 112 may be provided with one less input (or replaced by an inverter). In addition, the output of the comparator 122 may be coupled to a set input of a flip-flop 128. A Q output
25 of the flip-flop 128 may be coupled to a switch 130 (e.g., a MOSFET or bipolar transistor). The switch 130 is coupled across the capacitor C2. Thus, when the output of the comparator 122 changes to a logic high voltage, this sets the flip-flop 128 and closes the switch 130. As a result, the capacitor C2 begins to discharge through the switch 130. The capacitor C2 may be discharged during portions of the clock period used to control
30 switching. In a preferred embodiment, a time constant for discharging the capacitor C2 is such that the capacitor C2 may lose approximately one-third of its voltage level in a

single switching cycle. Thus, assuming the switch 130 is implemented by a transistor, the on-resistance relative to the value of the capacitor C2 is sufficient to provide this time constant. If needed, a resistor (not shown) may be coupled in series with the switch 130. A set input of the flip-flop 128 may be coupled to an output of the duty cycle limiter 116. Accordingly, the flip-flop 128 is reset at the beginning of the next cycle for the switch SW1. This opens the switch 130. As a result, the current source 126 begins to charge the capacitor C2.

Thus, in the event of a "hard" short in the load, in which the load impedance falls to nearly zero, the capacitor C2 will be discharged to nearly ground level within a few switching cycles. As a result, the duty cycle of the switch SW1 will be limited further by operation of the comparator 108 than by the comparator 122. In the event of a "soft short" in which the load impedance falls below expected levels, but not to zero, then the capacitor C2 will not be completely discharged. As a result, the duty cycle of the switch SW1 will be less limited than in the event of a hard short. Thus, under these conditions, the output voltage may continue to be regulated. It will be apparent, therefore, that the duty cycle of the switch SW1 (and the switch SW2) may be limited by an amount that is related to the level of the output current and, thus, the degree of the fault.

Figure 2 illustrates a schematic diagram of an alternate embodiment of a power converter 100' in accordance with an aspect of the present invention. As shown in Figure 2, the soft-start capacitor C2 and current source 126 of the duty cycle limiter of Figure 1 may be replaced with a counter 132 having its output coupled to a digital-to-analog converter 134. An output of the digital-to-analog converter 134 may be coupled to the input of comparator 108 in place of the signal Vss. Upon start-up, the counter 132 may begin counting (e.g., counting up from zero). When the output of the comparator 122 is a logic high voltage, the counter 132 may be reset to zero or to some other value in order to limit the duty cycle in the event of fault which causes an excessive output current. Alternately, during periods that the Q output of the flip-flop 128 is a logic high voltage, the counter 132 may be programmed to change the count gradually (e.g., by counting down). When the output of the analog to digital converter 134 goes beyond a limit set by the feedback signal VEAO, the output of the analog to digital converter 134 may control the duty cycle in accordance with the count.

Figures 3a and 3b illustrate a schematic diagram of a two-stage power factor correction and pulse width modulation power converter 100'' in accordance with an aspect of the present invention. The controller 104'' of Figure 3b differs from the controller 104 of Figure 1 and the controller 104' of Figure 2 principally in that the controller 104'' of Figure 3a includes a PFC section for controlling switching of a PFC stage of the converter 100'' of Figures 3a and 3b in addition to a pulse-width modulation (PWM) section. In addition, rather than using a resistive divider for sensing an output voltage V_o , as in Figures 1 and 2, the converter 100'' of Figures 3a and 3b may include a feedback arrangement 136 that having an optical isolator 138 for forming a signal VDC. The signal VDC is representative of a difference between the output voltage V_o and a desired level for the output voltage.

As shown in Figure 3a, an under-voltage lock out (UVLO) element 140 may maintain the voltage V_{ss} across the soft-start capacitor C2 at a low level when the controller 104'' does not have sufficient voltage at its V_{cc} supply for powering circuitry of the controller 104''. A comparator 142 may also maintain the voltage across the soft-start capacitor C2 at a low level when a voltage V_{in} developed by the PFC stage is below a predetermined level. Thus, the elements 140 and 142 ensure that the voltage across the capacitor C2 is not allowed to begin gradually increasing for start-up until the converter 100'' is appropriately conditioned to enter start-up mode. The elements 140 and 142 generally do not affect the switching duty cycle once start-up has commenced. Rather, as explained above, the duty cycle is generally adjusted in a closed feedback loop according to a level of the output voltage V_o , unless a fault occurs. When a fault occurs that results in an excessive current in the PWM stage, the comparator 122 may initiate the discharging phases of the capacitor C2, thereby reducing the switching duty cycle and, thus, the current. Further, a transistor 144 may be provided to limit the voltage across the capacitor C2.

Excessive current in the PWM stage of the converter 100'' of Figures 3a and 3b may be sensed via a voltage formed across resistor R20. The resistor R20 is coupled in series with the switch SW1. Accordingly, the current through the switch SW1 is sensed by forming a voltage across the resistor R20. A resistor R19 and a capacitor C17 are configured such that a current that is representative of the sensed current may charge the

capacitor C17 during each switching cycle. The capacitor C17 may be discharged once for each switching cycle by a transistor 146 which is coupled to receive the duty-limit signal from the duty cycle limiter 116. Accordingly, the voltage on the capacitor C17 may be used to form the ramp signal VRAMP which is applied to the comparator 108 for
5 controlling the switching duty cycle in the PWM stage. In addition, the voltage on the capacitor C17 may also be applied to the comparator 122 for determining whether the sensed current is excessive. More particularly, the comparator 122 compares the voltage across the capacitor (which is representative of the current through the switch SW1), to the reference level VREF2.

10 Figure 4 illustrates an exemplary embodiment of the three-input comparator 108 in accordance with an aspect of the present invention. A current source 148 may be coupled to a source of P-type transistors M1, M2 and M3. A drain of the transistor M1 may be coupled to a drain of an N-type transistor M4. Drains of the transistors M2 and M3 may be coupled together, to a drain of an N-type transistor M5 and to a gate of an N-
15 type transistor M6. A current source 150 may be coupled to a drain of the transistor M6. Sources of the transistors M4, M5 and M6 may be coupled to a ground node.

An inverting input Vn for the comparator 108 may be at the gate of transistor M1. A first non-inverting input Vp1 for the comparator 108 may be at the gate of transistor M2. A second non-inverting input Vp2 for the comparator 108 may be at the gate of the
20 transistor M3. Accordingly, referring to Figures 1-3, the signal VEO may be coupled to the gate of the transistor M1, the signal VRAMP may be coupled to the gate of the transistor M2 and the signal Vss may be coupled to the gate of the transistor M3. An output for the comparator 108 may be at the drain of the transistor M6. Accordingly, referred to Figures 1-3, the drain of the transistor M6 may be coupled to the logic gate
25 112.

The comparator 108 of Figure 4 is exemplary. Accordingly, it will be apparent that another embodiment of the comparator 108 may be used.

Figures 5a and 5b illustrate a schematic diagram of a two-stage power factor correction and pulse width modulation power converter in accordance with an aspect of
30 the present invention. An example of such a power converter is available under part

number CM6900 from Champion Microelectronic Corporation, located at 4020 Moorpark Avenue, Suite 105, San Jose, California.

Advantages of the invention include further limiting power dissipation in the event of an excessive current condition and an ability to continue to regulate the output voltage in the event of certain excessive current conditions.

Thus, while the foregoing has been with reference to particular embodiments of the invention, it will be appreciated by those skilled in the art that changes in these embodiments may be made without departing from the principles and spirit of the invention, the scope of which is defined by the appended claims.

What is claimed is:

- 1 1. A switching power converter for providing a load with an output current
2 and voltage, comprising:
3 a switch for transferring energy from a source to the load by opening and
4 closing the switch according to a duty cycle; and
5 a duty cycle limiter coupled to the switch wherein the duty cycle limiter is
6 triggered when the output current exceeds a predetermined level, the duty cycle
7 limiter including a capacitor having a charge that is gradually changed in response
8 to the output current exceeding the predetermined level and wherein the duty
9 cycle is related to a voltage on the capacitor.
- 1 2. The power converter according to claim 1, wherein a time constant for
2 changing the charge on the capacitor is such that a voltage across the capacitor is
3 changed by approximately one-third for each switching cycle that the duty cycle
4 limiter is triggered.
- 1 3. The power converter according to claim 1, further comprising a sensor for
2 sensing the output current.
- 1 4. The power converter according to claim 3, wherein the sensor is resistive.
- 1 5. The power converter according to claim 3, wherein the sensor is inductive.
- 1 6. The power converter according to claim 3, further comprising a
2 comparator for comparing the output current to the predetermined level wherein
3 the charge on the capacitor is changed according to an output of the comparator.

1 7. The power converter according to claim 1, wherein the capacitor is
2 charged by constant current source and discharged in response to the duty cycle
3 limiter being triggered.

1 8. The power converter according to claim 1, further comprising a
2 comparator for controlling the duty cycle of the switch by comparing a feedback
3 signal that is representative of the output voltage to a periodic ramp signal.

1 9. The power converter according to claim 8, wherein when the voltage
2 across the capacitor goes beyond a limit set by the feedback signal in response to
3 changing the charge on the capacitor, the voltage across the capacitor controls the
4 duty cycle.

1 10. The power converter according to claim 8, wherein the periodic ramp
2 signal is representative of the output current.

1 11. The power converter according to claim 10, wherein the duty cycle limiter
2 is triggered when the periodic ramp signal exceeds a predetermined level.

1 12. The power converter according to claim 1, wherein the duty cycle limiter
2 provides a soft-start in which the switching duty cycle is gradually increased upon
3 power-up.

1 13. A switching power converter for providing a load with an output current
2 and voltage comprising a switch for transferring energy from a source to the load
3 by opening and closing the switch according to a duty cycle wherein when the
4 output current reaches an excessive level, the duty cycle is limited to an amount
5 that is related to a degree to which the output current is excessive.

- 1 14. The power converter according to claim 13, further comprising a duty
2 cycle limiter that is triggered when the output current exceeds a predetermined
3 level.
- 1 15. The power converter according to claim 14, wherein the duty cycle limiter
2 comprises a capacitor in which a charge on the capacitor is gradually changed
3 when the duty cycle limiter is triggered and wherein the duty cycle is related to a
4 voltage on the capacitor.
- 1 16. The power converter according to claim 14, wherein the duty cycle limiter
2 comprises a counter that initiated to count when the duty cycle limiter is triggered
3 and wherein the duty cycle is related to a count of the counter.
- 1 17. A switching power converter for providing a load with an output current
2 and voltage, comprising
3 a switch for transferring energy from a source to the load by opening and
4 closing the switch according to a duty cycle; and
5 a duty cycle limiter coupled to the switch wherein the duty cycle limiter is
6 triggered when the output current exceeds a predetermined level, the duty cycle
7 limiter including a counter and wherein the duty cycle is related to a count of the
8 counter.
- 1 18. The power converter according to claim 17, wherein a count of counter is
2 gradually changed in response to the duty cycle limiter being triggered.
- 1 19. The power converter according to claim 18, further comprising a sensor
2 for sensing the output current.
- 1 20. The power converter according to claim 19, wherein the sensor is
2 resistive.

1 21. The power converter according to claim 19, wherein the sensor is
2 inductive.

1 22. The power converter according to claim 19, further comprising a
2 comparator for comparing the output current to the predetermined level wherein
3 the counter is initiated to count according to an output of the comparator.

1 23. The power converter according to claim 18, further comprising a
2 comparator for controlling the duty cycle of the switch by comparing a feedback
3 signal that is representative of the output voltage to a periodic ramp signal.

1 24. The power converter according to claim 23, further comprising an analog
2 to digital converter for converting the count to a voltage and wherein when the
3 voltage at the digital to analog converter goes beyond a limit set by the feedback
4 signal, the voltage at the digital to analog converter controls the duty cycle.

1 25. The power converter according to claim 23, wherein the periodic ramp
2 signal is representative of the output current.

1 26. The power converter according to claim 25, wherein the duty cycle limiter
2 is triggered when the periodic ramp signal exceeds a predetermined level.

1 27. The power converter according to claim 17, wherein the duty cycle limiter
2 provides a soft-start in which the switching duty cycle is gradually increased upon
3 power-up.

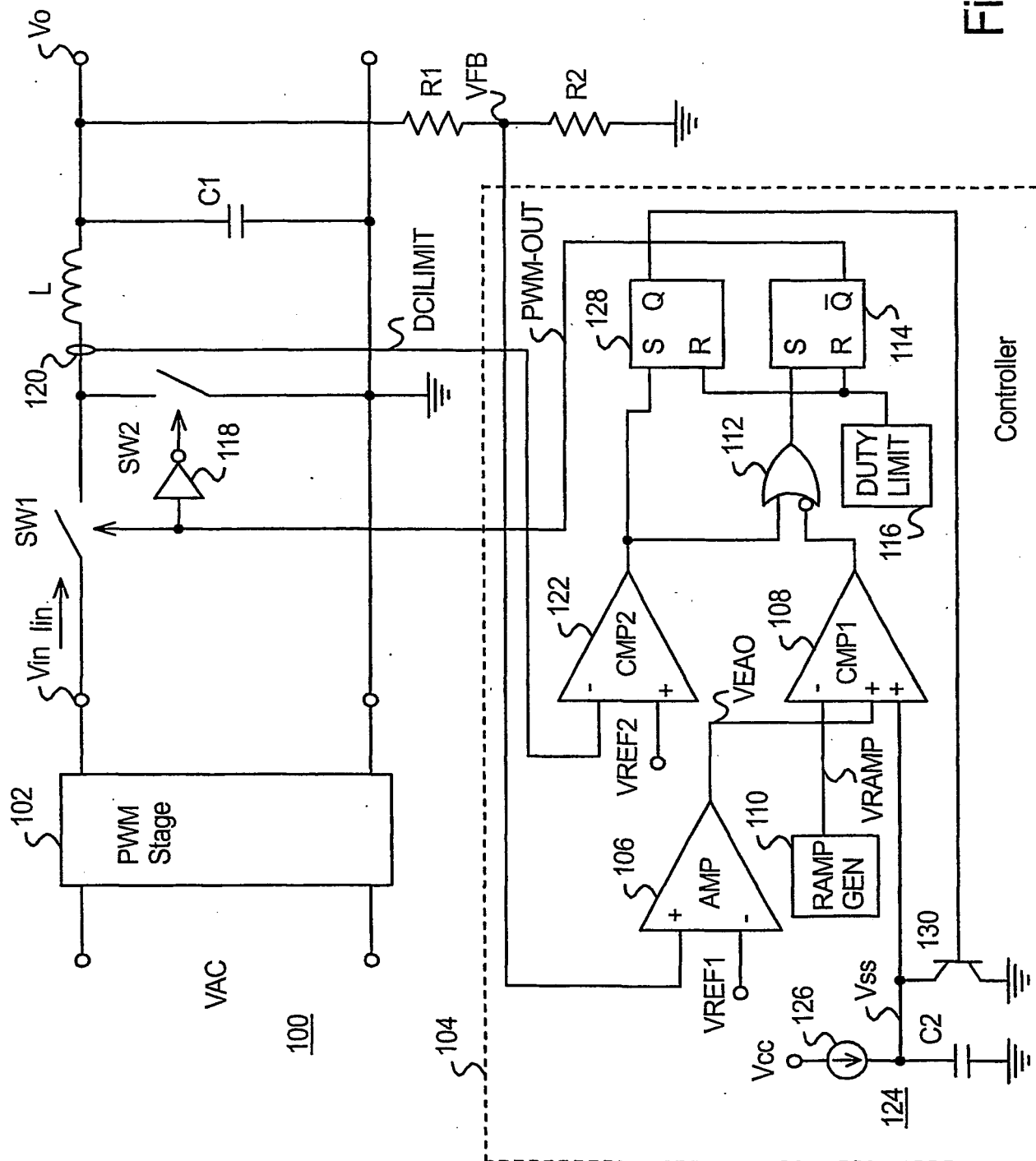


Fig. 1

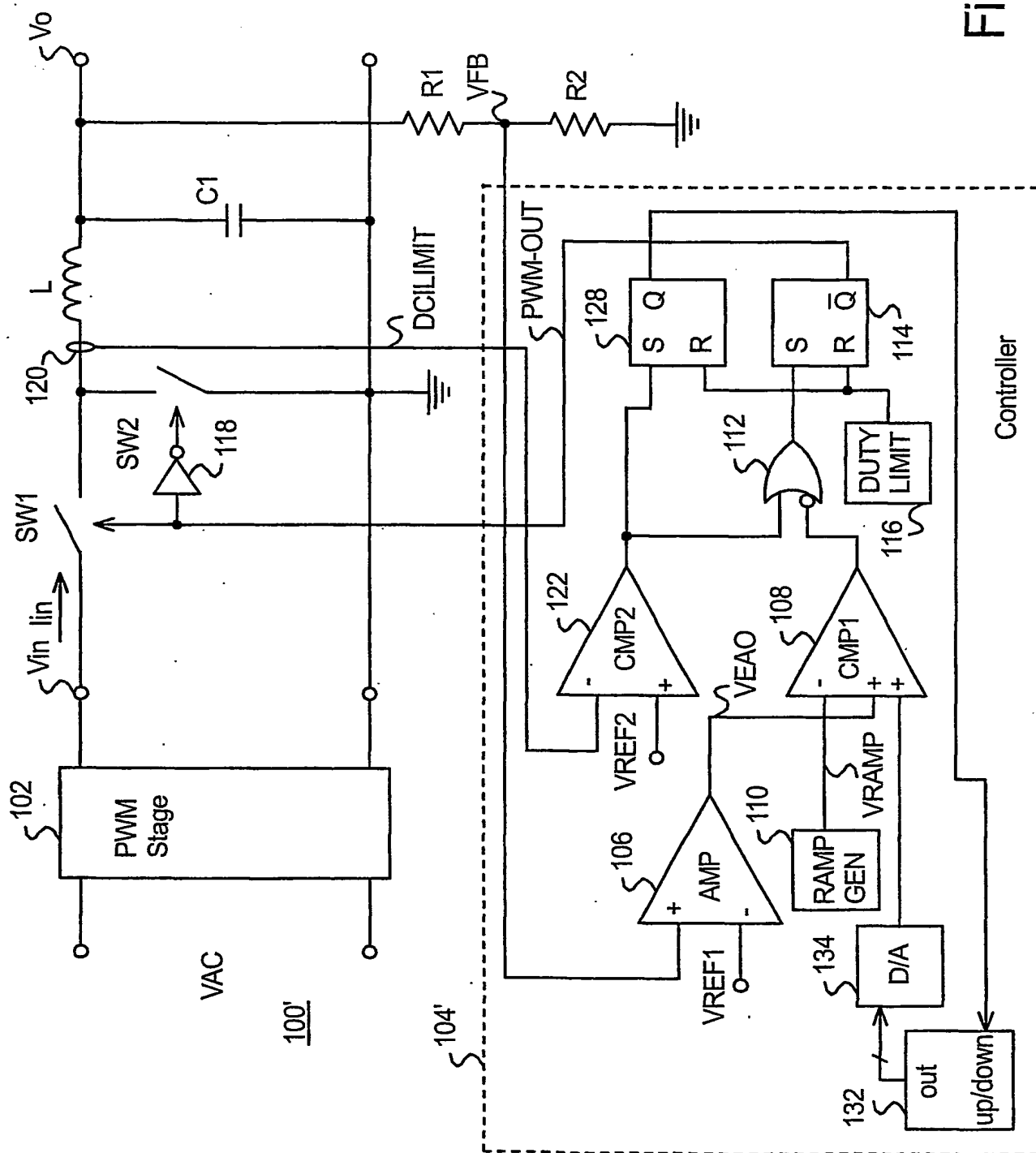


Fig. 2

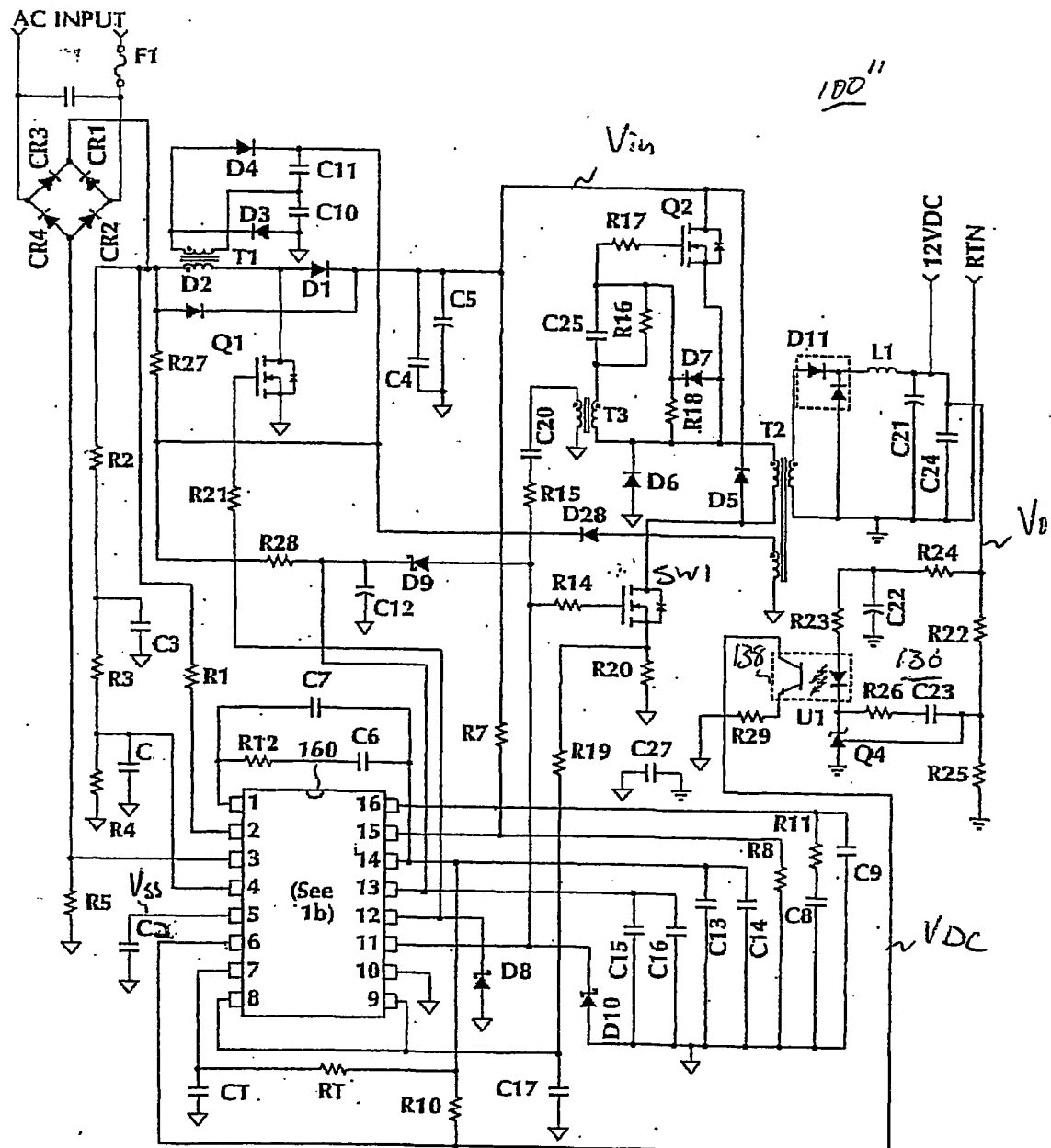


Figure 3a

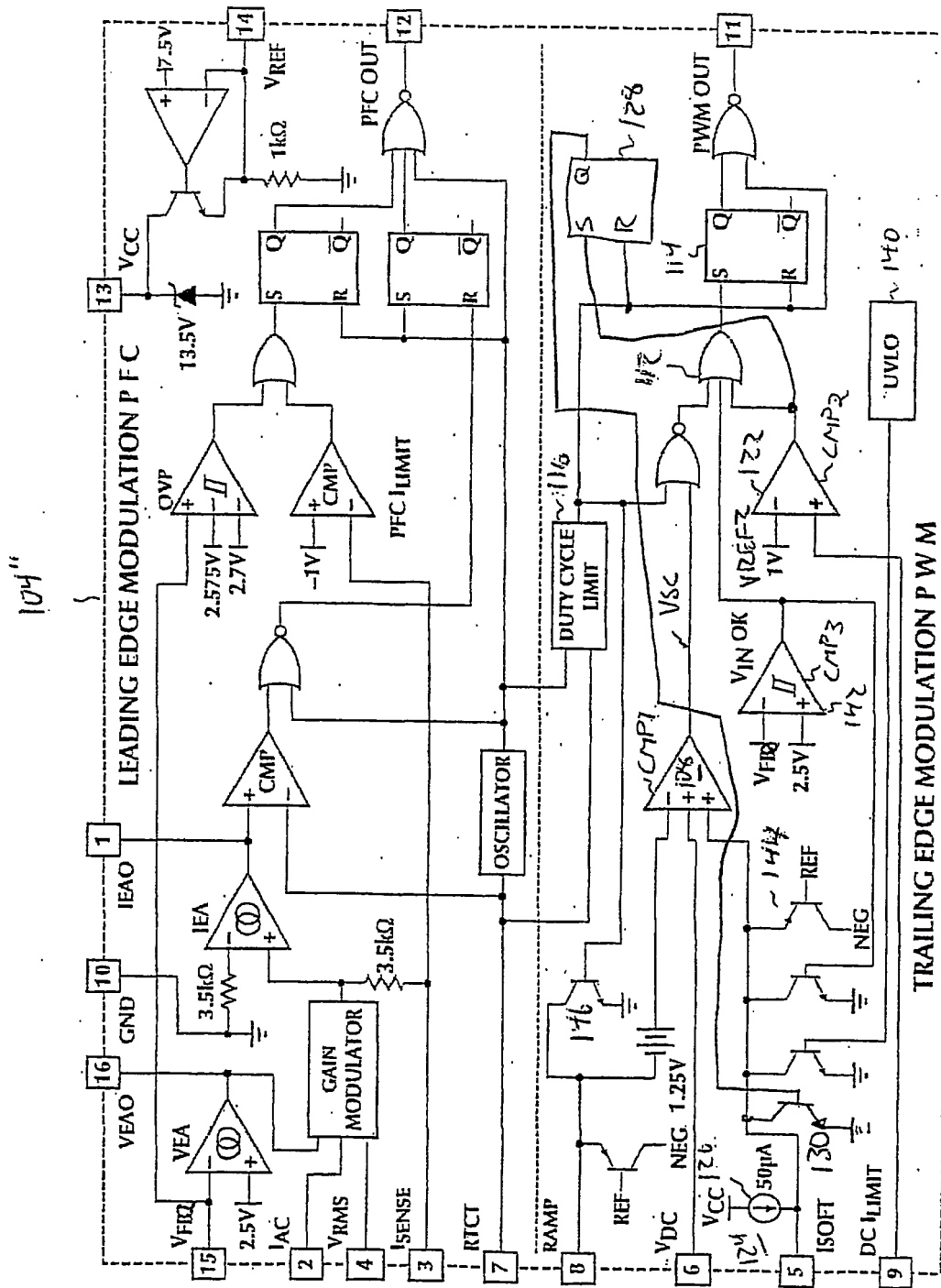


Figure 3b

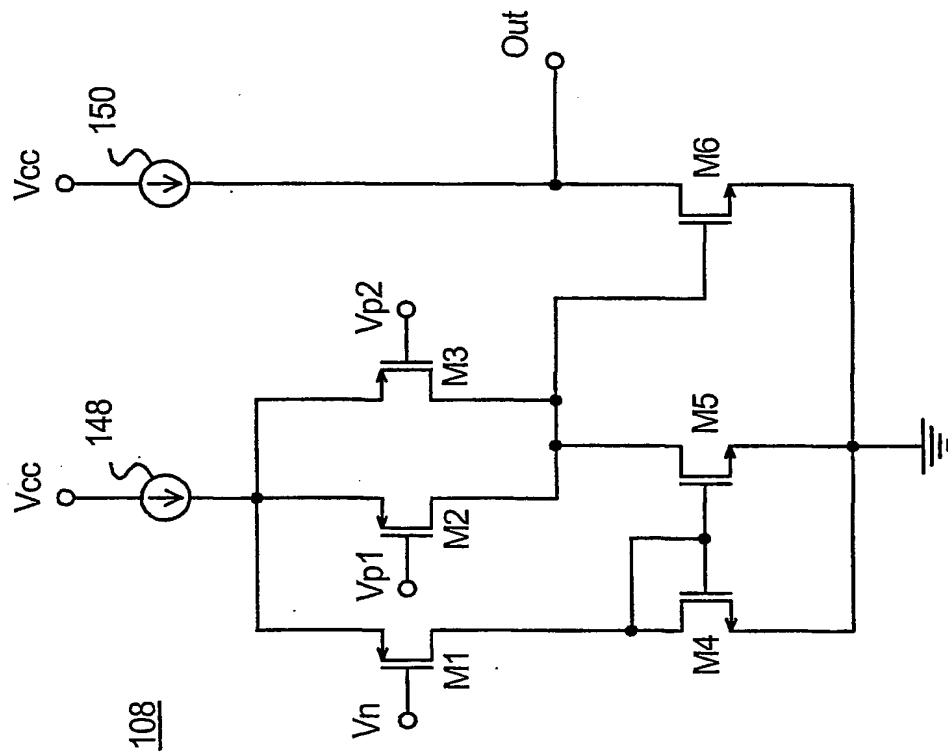
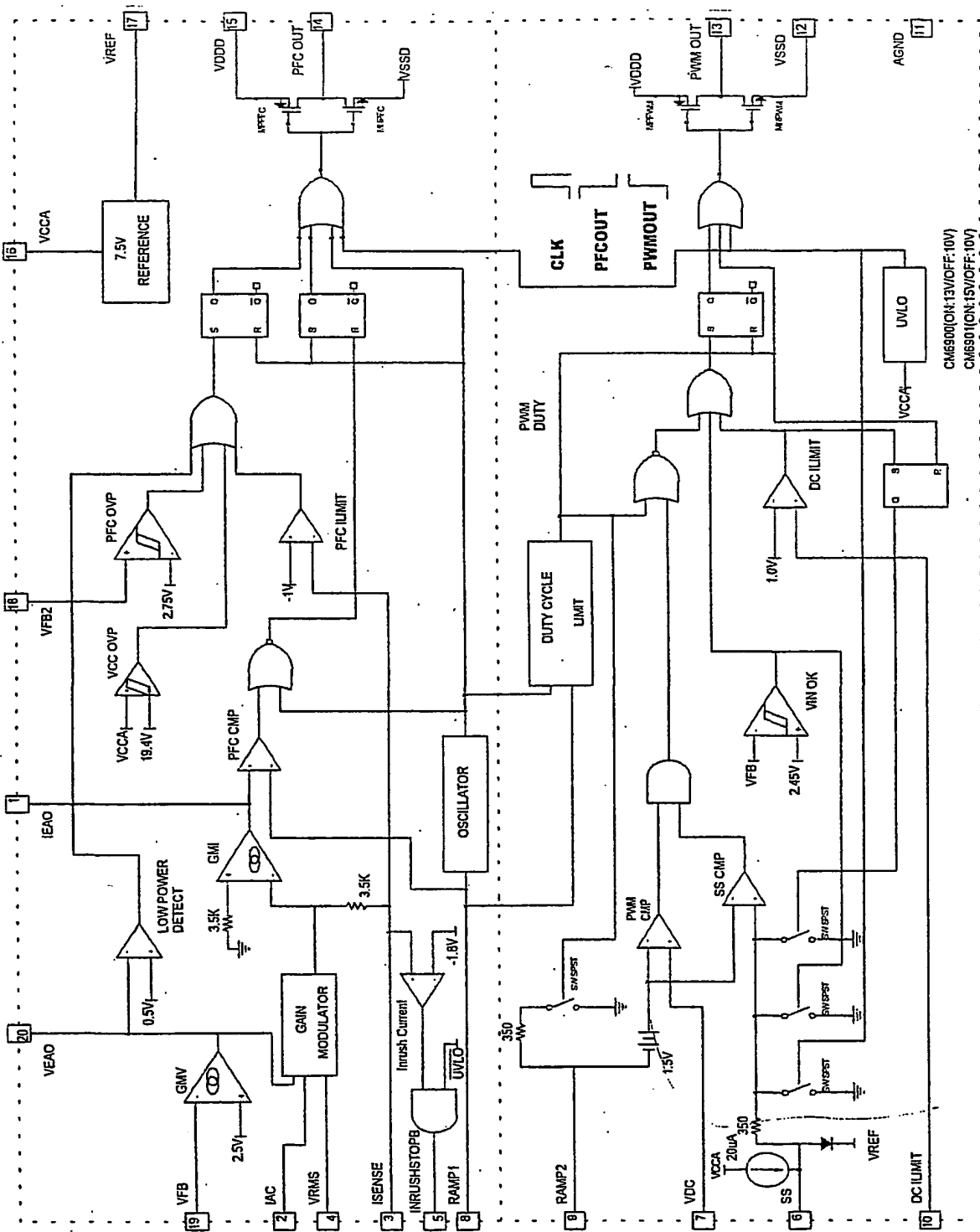
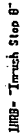


Fig. 4





56
C. H.

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US02/19890

A. CLASSIFICATION OF SUBJECT MATTER

IPC(7) : G05F 1/46, 1/56, 1/565, 1/573

US CL : 323/282, 283, 284, 351

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 323/282, 283, 284, 351

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
NONE

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

NONE

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 4,754,388 A (POSPISIL) 28 June 1988 (28.06.1988), col. 4, line 46 to col.5, line 25.	1-27
X	US 5,859,527 A (COOK) 12 January 1999 (12.01.1999), see entire document.	1-27
A,P	US 6,346,778 B1 (MASON et al.) 12 February 2002 (12.02.2002), see entire document.	1, 13 and 17



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:	"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A" document defining the general state of the art which is not considered to be of particular relevance	"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E" earlier document published on or after the international filing date	"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"G" document member of the same patent family
"O" document referring to an oral disclosure, use, exhibition or other means	
"P" document published prior to the international filing date but later than the priority date claimed	

Date of the actual completion of the international search

29 AUGUST 2002

Date of mailing of the international search report

30 SEP 2002

Name and mailing address of the ISA/US
Commissioner of Patents and Trademarks
Box PCT
Washington, D.C. 20231

Facsimile No. (703) 305-3230

Authorized officer

ADOLF BERHANE

Telephone No. (703) 308-3299

CORRECTED VERSION

(19) World Intellectual Property
Organization
International Bureau



(43) International Publication Date
3 January 2003 (03.01.2003)

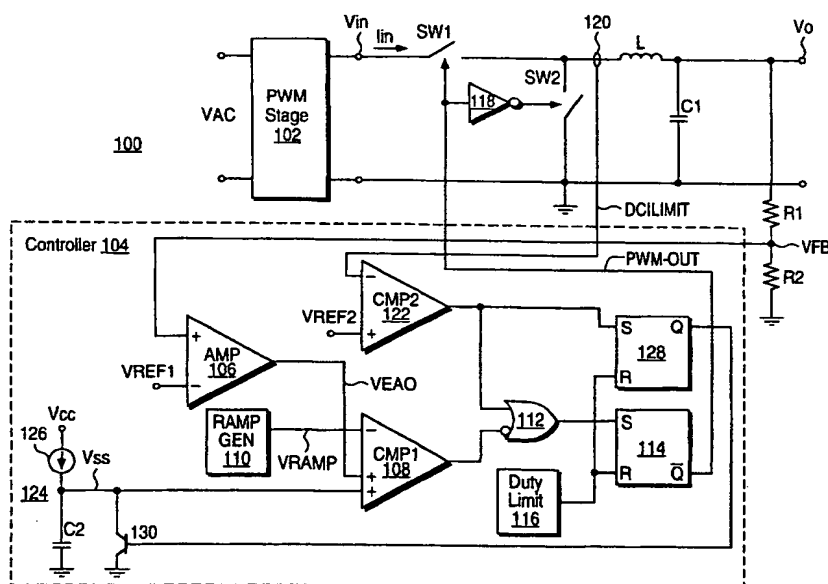
PCT

(10) International Publication Number
WO 2003/001314 A1

- (51) International Patent Classification⁷: G05F 1/46, 1/56, 1/565, 1/573
- (21) International Application Number: PCT/US2002/019890
- (22) International Filing Date: 21 June 2002 (21.06.2002)
- (25) Filing Language: English
- (26) Publication Language: English
- (30) Priority Data:
60/300,492 21 June 2001 (21.06.2001) US
10/177,557 21 June 2001 (21.06.2001) US
- (71) Applicant (for all designated States except US): CHAMPION MICROELECTRONIC CORP. [US/US]; 4020 Moorpark Avenue, Suite 105, San Jose, CA 95117 (US).
- (72) Inventor; and
- (75) Inventor/Applicant (for US only): HWANG, Jeffrey [US/US]; 20576 Manor Drive, Saratoga, CA 95070 (US).
- (74) Agent: WESTBERG, Derick, J.; Law Offices of Derek J. Westberg, 2 N. Second Street, Suite 1390, San Jose, CA 95113 (US).
- (81) Designated States (national): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, OM, PH, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VN, YU, ZA, ZM, ZW.
- (84) Designated States (regional): ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).
- Published: — with international search report

[Continued on next page]

(54) Title: CURRENT LIMITING TECHNIQUE FOR A SWITCHING POWER CONVERTER



(57) Abstract: An improved technique for limiting current in a switching power converter (100). The switching power converter includes a soft-start circuit (104) which slowly increases a switching duty cycle upon power-up. Once the converter is operating normally, the duty cycle is controlled to regulate the output voltage. In the event an excessive output current is detected, soft-start circuit is controlled to reduce the switching duty cycle. More particularly, a soft-start capacitor may be discharged during portions of a clock period used to control switching.

WO 2003/001314 A1



(48) Date of publication of this corrected version:

19 February 2004

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(15) Information about Correction:

see PCT Gazette No. 08/2004 of 19 February 2004, Section II

CURRENT LIMITING TECHNIQUE FOR A SWITCHING POWER CONVERTER

This application claims the benefit of U.S. Provisional Application Serial No.
5 60/300,492, filed June 21, 2001.

Field of the Invention:

The invention relates to switching power converters. More particularly, the
invention relates to a technique for limiting current by limiting a switching duty cycle in
10 such a power converter.

Background of the Invention:

In a conventional switching power converter, provision may be made for limiting
current to a load in the event the load experiences a fault. For example, U.S. Patent No.
15 5,742,151 discloses a PFC-PWM power converter in which the output current developed
by the PWM section is limited in when an excessive output current is detected. More
particularly, for each switch cycle, the switch is closed upon sensing an excessive output
current. A drawback to this technique is that when the switch is opened for each
switching cycle, an excessive current can occur before the switch is closed in response to
20 the excessive current. This repeated occurrence of excessive current may cause excessive
power dissipation in the converter.

What is needed is an improved current limiting technique for a switching power
converter. It is to these ends that the present invention is directed.

25 Summary of the Invention:

The present invention is an improved technique for limiting current in a switching
power converter. The power converter includes a switch for transferring energy from a
source to the load by opening and closing the switch according to a duty cycle. A duty
cycle limiter is triggered when the output current of the converter exceeds a
30 predetermined level. The duty cycle is limited to an amount that is related to a degree to
which the output current is excessive. In one aspect, the duty cycle limiter include a

capacitor having a charge that is gradually changed in response to the output current exceeding the predetermined level where the duty cycle is related to a voltage on the capacitor. In another aspect, the duty cycle limiter includes a counter where the duty cycle is related to a count of the counter. In another aspect, the duty cycle limiter
5 provides a soft-start in which the switching duty cycle is gradually increased upon power-up. Once the converter is operating normally, the duty cycle is controlled to regulate the output voltage.

The invention has an advantage in that by reducing the switching duty cycle, the output current is reduced and is, thus, less likely to reach an excessive level upon each
10 cycle of the switch. In comparisons to prior techniques, this reduces power dissipation in the converter.

Brief Description of the Drawings:

Figure 1 illustrates a schematic diagram of a power converter in accordance with
15 an aspect of the present invention;

Figure 2 illustrates a schematic diagram of an alternate embodiment of a power converter in accordance with an aspect of the present invention;

Figures 3a and 3b illustrate a schematic diagram of a two-stage power factor correction and pulse width modulation power converter in accordance with an aspect of
20 the present invention;

Figure 4 illustrates an exemplary three-input comparator that may be used with the power converters of the present invention; and

Figures 5a and 5b illustrate a schematic diagram of a two-stage power factor correction and pulse width modulation power converter in accordance with an aspect of
25 the present invention.

Detailed Description of a Preferred Embodiment:

Figure 1 illustrates a schematic diagram of a power converter 100 in accordance with an aspect of the present invention. An input voltage V_{in} may be applied to a first
30 terminal of a main power switch SW1 (e.g., a transistor switch). A second terminal of the switch SW1 may be coupled to a first terminal of a second switch SW2 (e.g., a transistor

switch) and to a first terminal of an inductor L. A second terminal of the inductor L may be coupled to a first terminal of a capacitor C1. A second terminal of the switch SW2 and a second terminal of the capacitor C1 may be coupled to a ground node. It will be apparent that the switch SW2 may be replaced by a diode.

5 A source 102 of the input voltage V_{in} may include a power factor correction (PFC) stage of the power converter 100. Thus, the source 102 may receive an alternating current (AC) signal and perform power factor correction in which current drawn from AC source VAC is maintained substantially in phase with the AC voltage signal so as to present a resistive load to the AC source. It will be apparent, however, that the PFC stage
10 may be omitted, in which case, the input voltage V_{in} may be provided by another source that provides a regulated voltage, an unregulated voltage or a loosely-regulated voltage.

 When the switch SW1 is closed, the switch SW2 is open. Under these conditions, current I_{in} from the source 102 charges the inductor L with energy. When the switch SW1 is opened, the switch SW2 is closed. Under these conditions, energy from the
15 inductor L charges the capacitor C1 with energy. An output voltage V_o formed across the capacitor C1 may be used to power a load (not shown). The level of power delivered to the load may be adjusted according to the duty cycle of the switches SW1 and SW2.

 A controller 104 may control the duty cycle of the switches SW1 and SW2 so as to maintain the output voltage V_o at a desired level. For this purpose, a first terminal of a
20 resistor R1 may be coupled to receive the output voltage V_o . A second terminal of the resistor R1 may be coupled to a first terminal of a resistor R2. A second terminal of the resistor R2 may be coupled to a ground node. Accordingly, the resistors R1 and R2 form a resistive divider in which a feedback signal VFB formed at an intermediate node of the resistive divider is representative of the level of the output voltage V_o .

25 The feedback signal VFB may be coupled to a first input terminal of an amplifier 106. Reference voltage V_{REF1} that is representative of a desired level for the output voltage V_o may be coupled to a second input of the amplifier 106. Accordingly, an output of the amplifier 106 forms an error signal VEAO that is representative of a difference between the output voltage V_o and a desired level for the output voltage. The
30 error signal VEAO may be coupled to a first input of a comparator 108. A second input

of the comparator 108 may be coupled to receive a periodic ramp signal VRAMP from a ramp generator 110.

The output of the comparator 108 forms a switch control signal VSC. When the level of the ramp signal VRAMP is below the level of the error signal VEAO, the switch control signal VSC may be a logic high voltage. Then, as the ramp signal rises, it eventually exceeds the level of the error signal VEAO. In response, the switch control signal VSC may transition to a logic low voltage until the ramp signal VRAMP is reset and the process repeats. Thus, the duty cycle of the switch control signal VSC is adjusted depending upon the level of the output voltage V_o .

The switch control signal VSC may be coupled to a first (inverting) input of a logic OR gate 112. An output of the logic gate 112 may be coupled to a set input S of a flip-flop or latch 114. A reset input R of the flip-flop 114 may be coupled to receive a periodic clock signal from a duty-cycle limiter 116. A \overline{Q} (inverted) output PWM-OUT of the flip-flop 114 may be coupled to control the switch SW1 and the switch SW2 (via an inverter 118).

When the flip-flop 114 is reset by the duty-cycle limiter 116, the switch SW1 is closed and the switch SW2 is opened. In addition, the ramp signal VRAMP, being synchronized with the periodic clock signal from the duty-cycle limiter 116, is reset to its initial value from which it begins to rise. Under these conditions, the switch control signal VSC is a logic high voltage and the output of the logic gate 112 is a logic low voltage. Then, when the level of the ramp signal VRAMP exceeds the level of the error signal VEAO, the switch control signal VSC transitions to a logic low voltage. As a result, the flip-flop 114 is set and the switch SW1 is opened and the switch SW2 is closed. The switch SW1 remains open and the switch SW2 remains closed until the flip-flop 114 is once again reset by the duty-cycle limiter 116.

The signal PWM-OUT may differ from the signal VSC in that the signal PWM-OUT may be duty-cycle limited by a duty cycle limiter 116. The duty cycle limiter 116 may form a periodic square wave signal whose duty cycle is equivalent to a maximum duty cycle allowed for the switch SW1.

When the output voltage V_o rises, the error signal VEAO also rises. As a result, the switch SW1 remains open for a longer portion of the switching cycle because more

time is required for the ramp signal VRAMP to exceed the error signal VEAO. Thus, the switching duty-cycle is reduced which tends to reduce the output voltage V_o .

Conversely, when the output voltage V_o falls, the error signal VEAO also falls. As a result, the switch SW1 remains open for a shorter portion of the switching cycle because
5 less time is required for the ramp signal to exceed the error signal VEAO. Thus, the switching duty-cycle is increased which tends to increase the output voltage V_o .
Accordingly, the output voltage V_o is regulated in a closed feedback loop.

The power converter 100 of Figure 1 is exemplary. Thus, it will be apparent that modifications can be made. For example, the exemplary power converter 100 uses
10 trailing-edge modulation, however, leading-edge modulation may be used. As another example, the power converter 100 has buck converter topology. However, another type of converter topology may be used, such as that of a boost converter.

A current sensor 120 may be coupled to sense current in the converter 100. As shown in Figure 1, the current sensor 120 may sense current in the inductor L.
15 Alternately, the current sensor 120 may sense current in the switch SW1 or the switch SW2. In either case, the current sensor 120 senses a current that is representative of an output current provided to the load. Further, the current sensor 120 may be implemented in a number of different ways. For example, a resistor that is configured to receive the current to be sensed forms a voltage that is representative of the current. As another
20 example, a current may be induced in the secondary winding of a transformer or coupled inductor. Thus, current in the inductor L may be sensed via an induced current in a second inductor (not shown) that is inductively coupled to the inductor L. Further, the current sensor 120 may form a signal that is representative of an average of the sensed current, such as by use of a filter.

25 The current sensor 120 forms a voltage signal DCILIMIT that is representative of the sensed current. This current-sensing signal may be coupled to a first input of a comparator 122. A second input of the comparator 122 may be coupled to receive a reference voltage VREF2 that is representative of a maximum desired level for the sensed current. An output of the comparator 122 may be coupled to a second input of the logic
30 OR gate 112. Thus, the output of the comparator 122 may open the switch SW1 in the event that a current sensing signal DCI LIMIT exceeds a predetermined level.

As explained above, under normal operating conditions, the comparator 108 compares a signal VFB that is representative of an output voltage V_o of the converter 100 to a periodic ramp signal VRAMP in order to adjust the duty cycle of the switch SW1. Accordingly, the output voltage V_o is regulated in a feedback loop.

5 Upon start-up, however, a duty cycle limiting circuit arrangement 124 may provide a soft-start in which the duty cycle of the switch SW1 is limited so as to prevent excessive current in the switch SW1. Thus, a soft-start voltage V_{ss} formed across a soft-start capacitor C2 is initially a low voltage level, when the output voltage V_o is significantly lower than the desired level. Over time, a current source 126 charges the
10 capacitor C2. Initially, when the signal V_{ss} is higher than the signal VEO, the voltage V_{ss} is compared by comparator 108 to the periodic ramp signal VRAMP. As the soft-start signal V_{ss} increases, so does the duty cycle of the switch SW1. As a result, the output voltage V_o increases. Once the level of VEO rises above the level of V_{ss} , then the comparator 108 compares the signal VFB to the ramp signal VRAMP to control the
15 duty cycle of the switch SW1. Accordingly, the comparator 108 compares the higher one of the two signals V_{ss} and VEO to the ramp signal VRAMP to control the duty cycle of the switch SW1.

The voltage signal DC ILIMIT is representative of the output current of a PWM stage of the converter 100 and is coupled to the comparator 122. In response to the signal
20 DC ILIMIT exceeding a predetermined level of the reference voltage VREF2 (e.g., 1.0 volt), the comparator 122 opens the switch SW1 via a logic OR gate 112. Optionally, the comparator 122 may be disconnected from the logic OR gate 112 and the logic OR gate 112 may be provided with one less input (or replaced by an inverter). In addition, the output of the comparator 122 may be coupled to a set input of a flip-flop 128. A Q output
25 of the flip-flop 128 may be coupled to a switch 130 (e.g., a MOSFET or bipolar transistor). The switch 130 is coupled across the capacitor C2. Thus, when the output of the comparator 122 changes to a logic high voltage, this sets the flip-flop 128 and closes the switch 130. As a result, the capacitor C2 begins to discharge through the switch 130. The capacitor C2 may be discharged during portions of the clock period used to control
30 switching. In a preferred embodiment, a time constant for discharging the capacitor C2 is such that the capacitor C2 may lose approximately one-third of its voltage level in a

single switching cycle. Thus, assuming the switch 130 is implemented by a transistor, the on-resistance relative to the value of the capacitor C2 is sufficient to provide this time constant. If needed, a resistor (not shown) may be coupled in series with the switch 130. A set input of the flip-flop 128 may be coupled to an output of the duty cycle limiter 116.

5 Accordingly, the flip-flop 128 is reset at the beginning of the next cycle for the switch SW1. This opens the switch 130. As a result, the current source 126 begins to charge the capacitor C2.

Thus, in the event of a "hard" short in the load, in which the load impedance falls to nearly zero, the capacitor C2 will be discharged to nearly ground level within a few
10 switching cycles. As a result, the duty cycle of the switch SW1 will be limited further by operation of the comparator 108 than by the comparator 122. In the event of a "soft short" in which the load impedance falls below expected levels, but not to zero, then the capacitor C2 will not be completely discharged. As a result, the duty cycle of the switch SW1 will be less limited than in the event of a hard short. Thus, under these conditions,
15 the output voltage may continue to be regulated. It will be apparent, therefore, that the duty cycle of the switch SW1 (and the switch SW2) may be limited by an amount that is related to the level of the output current and, thus, the degree of the fault.

Figure 2 illustrates a schematic diagram of an alternate embodiment of a power converter 100' in accordance with an aspect of the present invention. As shown in Figure
20 2, the soft-start capacitor C2 and current source 126 of the duty cycle limiter of Figure 1 may be replaced with a counter 132 having its output coupled to a digital-to-analog converter 134. An output of the digital-to-analog converter 134 may be coupled to the input of comparator 108 in place of the signal Vss. Upon start-up, the counter 132 may begin counting (e.g., counting up from zero). When the output of the comparator 122 is a
25 logic high voltage, the counter 132 may be reset to zero or to some other value in order to limit the duty cycle in the event of fault which causes an excessive output current. Alternately, during periods that the Q output of the flip-flop 128 is a logic high voltage, the counter 132 may be programmed to change the count gradually (e.g., by counting down). When the output of the analog to digital converter 134 goes beyond a limit set by
30 the feedback signal VEAO, the output of the analog to digital converter 134 may control the duty cycle in accordance with the count.

Figures 3a and 3b illustrate a schematic diagram of a two-stage power factor correction and pulse width modulation power converter 100'' in accordance with an aspect of the present invention. The controller 104'' of Figure 3b differs from the controller 104 of Figure 1 and the controller 104' of Figure 2 principally in that the controller 104'' of Figure 3a includes a PFC section for controlling switching of a PFC stage of the converter 100'' of Figures 3a and 3b in addition to a pulse-width modulation (PWM) section. In addition, rather than using a resistive divider for sensing an output voltage V_o , as in Figures 1 and 2, the converter 100'' of Figures 3a and 3b may include a feedback arrangement 136 that having an optical isolator 138 for forming a signal VDC. The signal VDC is representative of a difference between the output voltage V_o and a desired level for the output voltage.

As shown in Figure 3a, an under-voltage lock out (UVLO) element 140 may maintain the voltage V_{ss} across the soft-start capacitor C2 at a low level when the controller 104'' does not have sufficient voltage at its V_{cc} supply for powering circuitry of the controller 104''. A comparator 142 may also maintain the voltage across the soft-start capacitor C2 at a low level when a voltage V_{in} developed by the PFC stage is below a predetermined level. Thus, the elements 140 and 142 ensure that the voltage across the capacitor C2 is not allowed to begin gradually increasing for start-up until the converter 100'' is appropriately conditioned to enter start-up mode. The elements 140 and 142 generally do not affect the switching duty cycle once start-up has commenced. Rather, as explained above, the duty cycle is generally adjusted in a closed feedback loop according to a level of the output voltage V_o , unless a fault occurs. When a fault occurs that results in an excessive current in the PWM stage, the comparator 122 may initiate the discharging phases of the capacitor C2, thereby reducing the switching duty cycle and, thus, the current. Further, a transistor 144 may be provided to limit the voltage across the capacitor C2.

Excessive current in the PWM stage of the converter 100'' of Figures 3a and 3b may be sensed via a voltage formed across resistor R20. The resistor R20 is coupled in series with the switch SW1. Accordingly, the current through the switch SW1 is sensed by forming a voltage across the resistor R20. A resistor R19 and a capacitor C17 are configured such that a current that is representative of the sensed current may charge the

capacitor C17 during each switching cycle. The capacitor C17 may be discharged once for each switching cycle by a transistor 146 which is coupled to receive the duty-limit signal from the duty cycle limiter 116. Accordingly, the voltage on the capacitor C17 may be used to form the ramp signal VRAMP which is applied to the comparator 108 for controlling the switching duty cycle in the PWM stage. In addition, the voltage on the capacitor C17 may also be applied to the comparator 122 for determining whether the sensed current is excessive. More particularly, the comparator 122 compares the voltage across the capacitor (which is representative of the current through the switch SW1), to the reference level VREF2.

Figure 4 illustrates an exemplary embodiment of the three-input comparator 108 in accordance with an aspect of the present invention. A current source 148 may be coupled to a source of P-type transistors M1, M2 and M3. A drain of the transistor M1 may be coupled to a drain of an N-type transistor M4. Drains of the transistors M2 and M3 may be coupled together, to a drain of an N-type transistor M5 and to a gate of an N-type transistor M6. A current source 150 may be coupled to a drain of the transistor M6. Sources of the transistors M4, M5 and M6 may be coupled to a ground node.

An inverting input Vn for the comparator 108 may be at the gate of transistor M1. A first non-inverting input Vp1 for the comparator 108 may be at the gate of transistor M2. A second non-inverting input Vp2 for the comparator 108 may be at the gate of the transistor M3. Accordingly, referring to Figures 1-3, the signal VEAO may be coupled to the gate of the transistor M1, the signal VRAMP may be coupled to the gate of the transistor M2 and the signal Vss may be coupled to the gate of the transistor M3. An output for the comparator 108 may be at the drain of the transistor M6. Accordingly, referred to Figures 1-3, the drain of the transistor M6 may be coupled to the logic gate 112.

The comparator 108 of Figure 4 is exemplary. Accordingly, it will be apparent that another embodiment of the comparator 108 may be used.

Figures 5a and 5b illustrate a schematic diagram of a two-stage power factor correction and pulse width modulation power converter in accordance with an aspect of the present invention. An example of such a power converter is available under part

number CM6900 from Champion Microelectronic Corporation, located at 4020 Moorpark Avenue, Suite 105, San Jose, California.

Advantages of the invention include further limiting power dissipation in the event of an excessive current condition and an ability to continue to regulate the output voltage in the event of certain excessive current conditions.

Thus, while the foregoing has been with reference to particular embodiments of the invention, it will be appreciated by those skilled in the art that changes in these embodiments may be made without departing from the principles and spirit of the invention, the scope of which is defined by the appended claims.

What is claimed is:

- 1 1. A switching power converter for providing a load with an output current
2 and voltage, comprising:
3 a switch for transferring energy from a source to the load by opening and
4 closing the switch according to a duty cycle; and
5 a duty cycle limiter coupled to the switch wherein the duty cycle limiter is
6 triggered when the output current exceeds a predetermined level, the duty cycle
7 limiter including a capacitor having a charge that is gradually changed in response
8 to the output current exceeding the predetermined level and wherein the duty
9 cycle is related to a voltage on the capacitor.
- 1 2. The power converter according to claim 1, wherein a time constant for
2 changing the charge on the capacitor is such that a voltage across the capacitor is
3 changed by approximately one-third for each switching cycle that the duty cycle
4 limiter is triggered.
- 1 3. The power converter according to claim 1, further comprising a sensor for
2 sensing the output current.
- 1 4. The power converter according to claim 3, wherein the sensor is resistive.
- 1 5. The power converter according to claim 3, wherein the sensor is inductive.
- 1 6. The power converter according to claim 3, further comprising a
2 comparator for comparing the output current to the predetermined level wherein
3 the charge on the capacitor is changed according to an output of the comparator.

1 7. The power converter according to claim 1, wherein the capacitor is
2 charged by constant current source and discharged in response to the duty cycle
3 limiter being triggered.

1 8. The power converter according to claim 1, further comprising a
2 comparator for controlling the duty cycle of the switch by comparing a feedback
3 signal that is representative of the output voltage to a periodic ramp signal.

1 9. The power converter according to claim 8, wherein when the voltage
2 across the capacitor goes beyond a limit set by the feedback signal in response to
3 changing the charge on the capacitor, the voltage across the capacitor controls the
4 duty cycle.

1 10. The power converter according to claim 8, wherein the periodic ramp
2 signal is representative of the output current.

1 11. The power converter according to claim 10, wherein the duty cycle limiter
2 is triggered when the periodic ramp signal exceeds a predetermined level.

1 12. The power converter according to claim 1, wherein the duty cycle limiter
2 provides a soft-start in which the switching duty cycle is gradually increased upon
3 power-up.

1 13. A switching power converter for providing a load with an output current
2 and voltage comprising a switch for transferring energy from a source to the load
3 by opening and closing the switch according to a duty cycle wherein when the
4 output current reaches an excessive level, the duty cycle is limited to an amount
5 that is related to a degree to which the output current is excessive.

- 1 14. The power converter according to claim 13, further comprising a duty
2 cycle limiter that is triggered when the output current exceeds a predetermined
3 level.
- 1 15. The power converter according to claim 14, wherein the duty cycle limiter
2 comprises a capacitor in which a charge on the capacitor is gradually changed
3 when the duty cycle limiter is triggered and wherein the duty cycle is related to a
4 voltage on the capacitor.
- 1 16. The power converter according to claim 14, wherein the duty cycle limiter
2 comprises a counter that initiated to count when the duty cycle limiter is triggered
3 and wherein the duty cycle is related to a count of the counter.
- 1 17. A switching power converter for providing a load with an output current
2 and voltage, comprising
3 a switch for transferring energy from a source to the load by opening and
4 closing the switch according to a duty cycle; and
5 a duty cycle limiter coupled to the switch wherein the duty cycle limiter is
6 triggered when the output current exceeds a predetermined level, the duty cycle
7 limiter including a counter and wherein the duty cycle is related to a count of the
8 counter.
- 1 18. The power converter according to claim 17, wherein a count of counter is
2 gradually changed in response to the duty cycle limiter being triggered.
- 1 19. The power converter according to claim 18, further comprising a sensor
2 for sensing the output current.
- 1 20. The power converter according to claim 19, wherein the sensor is
2 resistive.

1 21. The power converter according to claim 19, wherein the sensor is
2 inductive.

1 22. The power converter according to claim 19, further comprising a
2 comparator for comparing the output current to the predetermined level wherein
3 the counter is initiated to count according to an output of the comparator.

1 23. The power converter according to claim 18, further comprising a
2 comparator for controlling the duty cycle of the switch by comparing a feedback
3 signal that is representative of the output voltage to a periodic ramp signal.

1 24. The power converter according to claim 23, further comprising an analog
2 to digital converter for converting the count to a voltage and wherein when the
3 voltage at the digital to analog converter goes beyond a limit set by the feedback
4 signal, the voltage at the digital to analog converter controls the duty cycle.

1 25. The power converter according to claim 23, wherein the periodic ramp
2 signal is representative of the output current.

1 26. The power converter according to claim 25, wherein the duty cycle limiter
2 is triggered when the periodic ramp signal exceeds a predetermined level.

1 27. The power converter according to claim 17, wherein the duty cycle limiter
2 provides a soft-start in which the switching duty cycle is gradually increased upon
3 power-up.

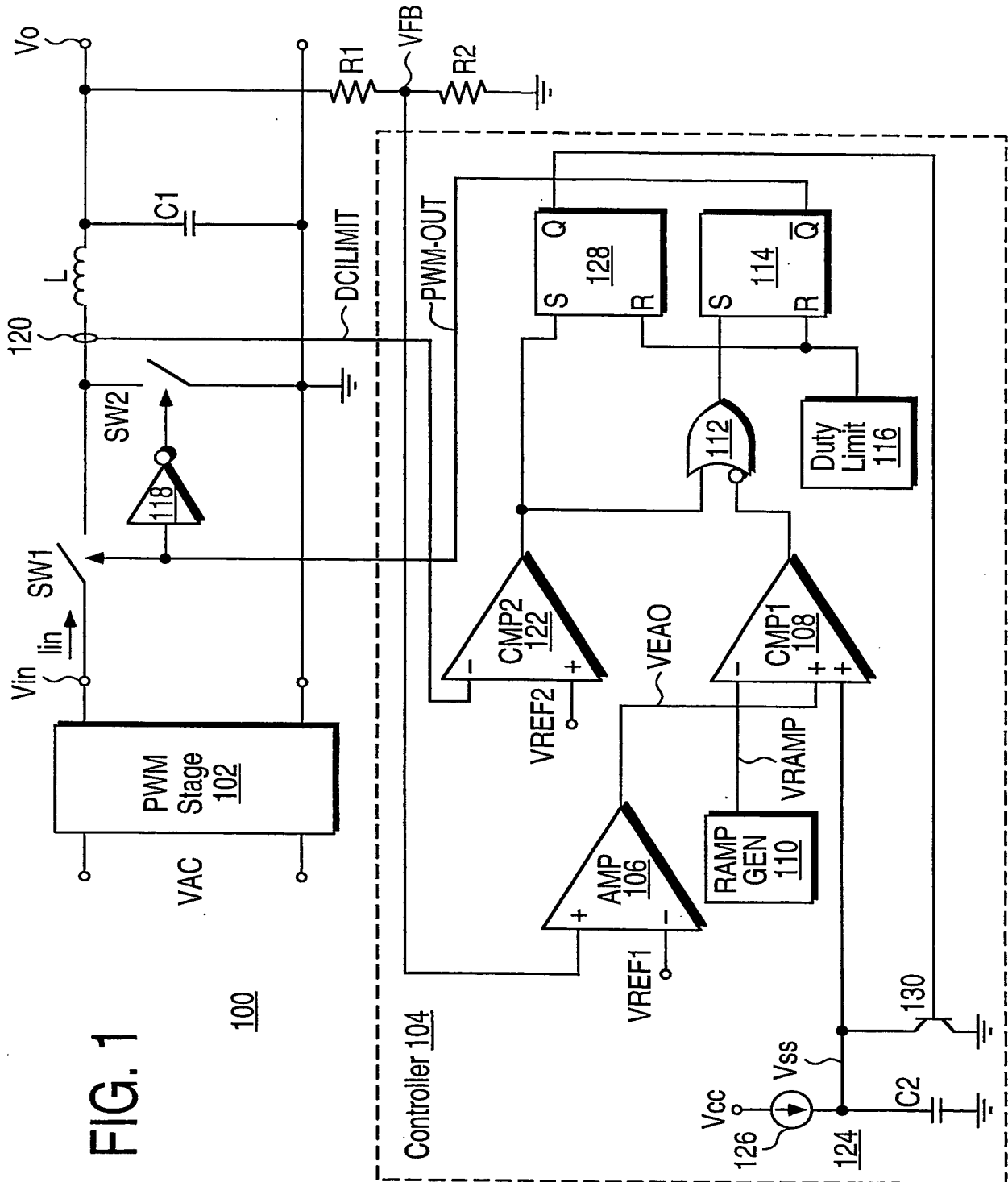


FIG. 1

2/9

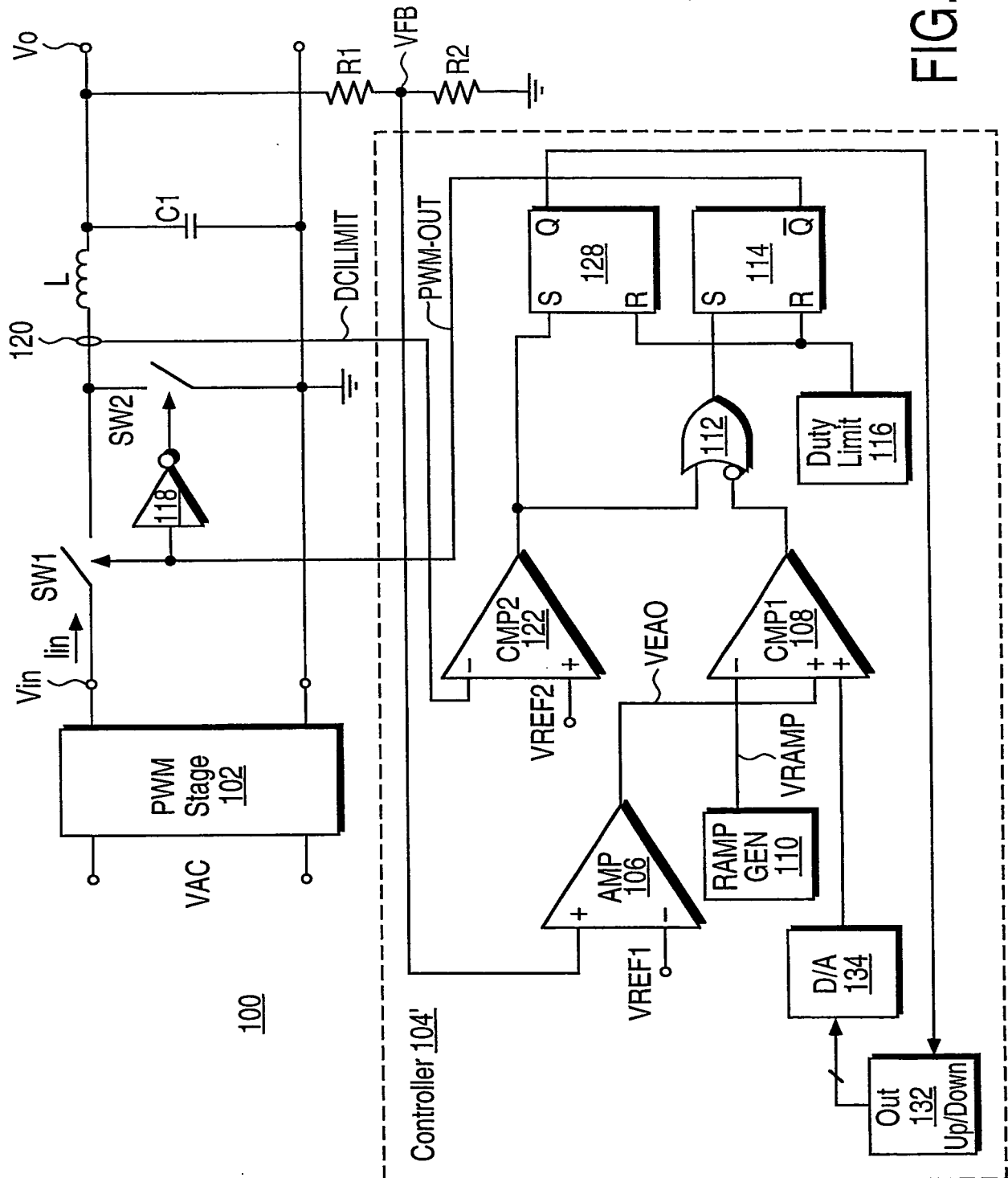


FIG. 2

3/9

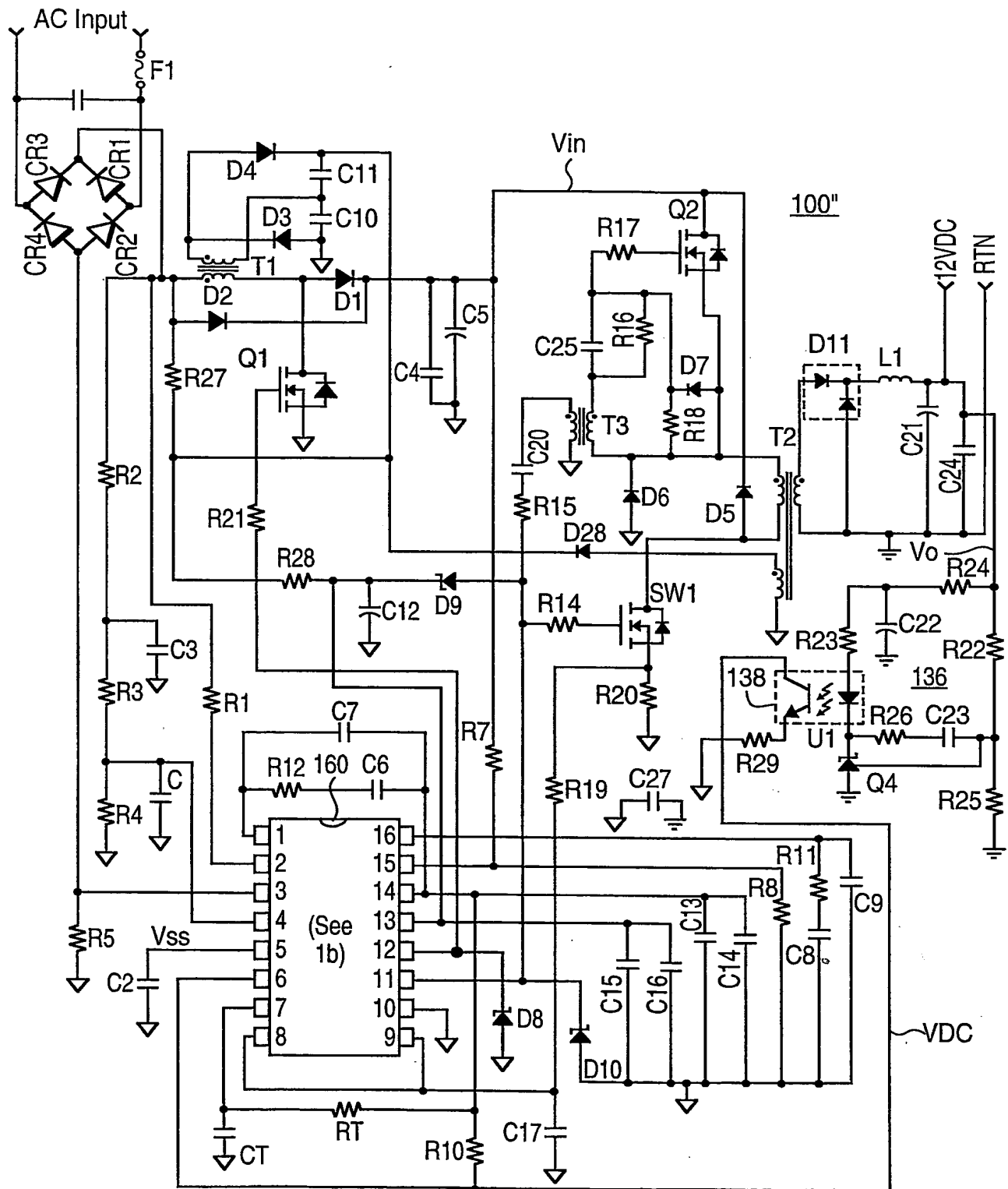


FIG. 3A

SUBSTITUTE SHEET (RULE 26)

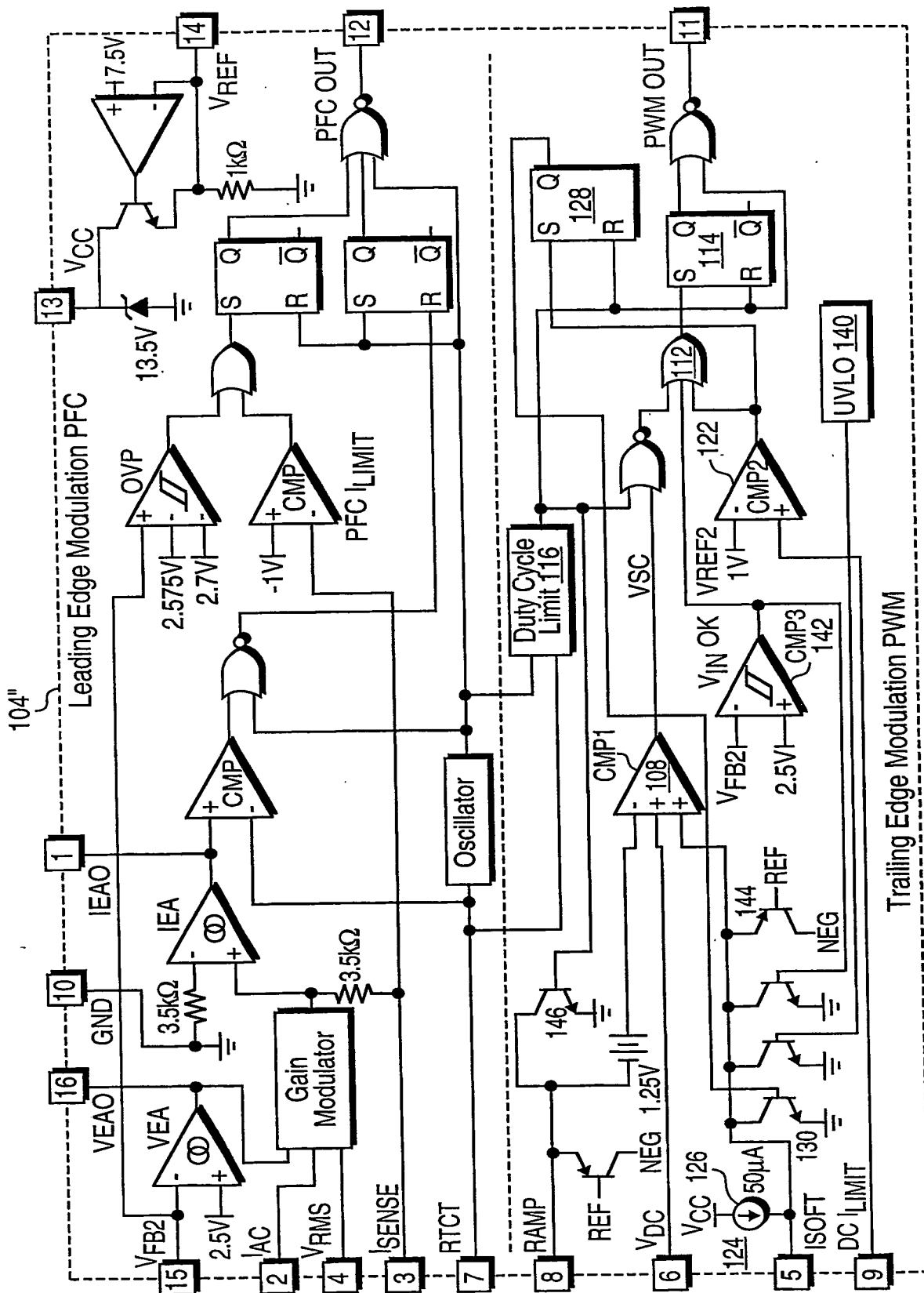


FIG. 3B

5/9

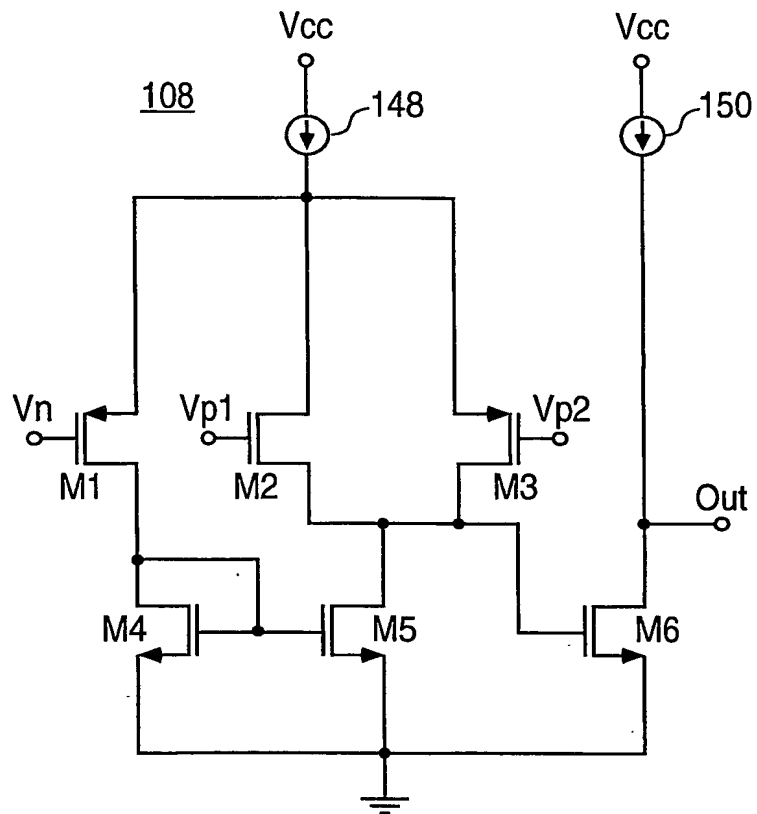
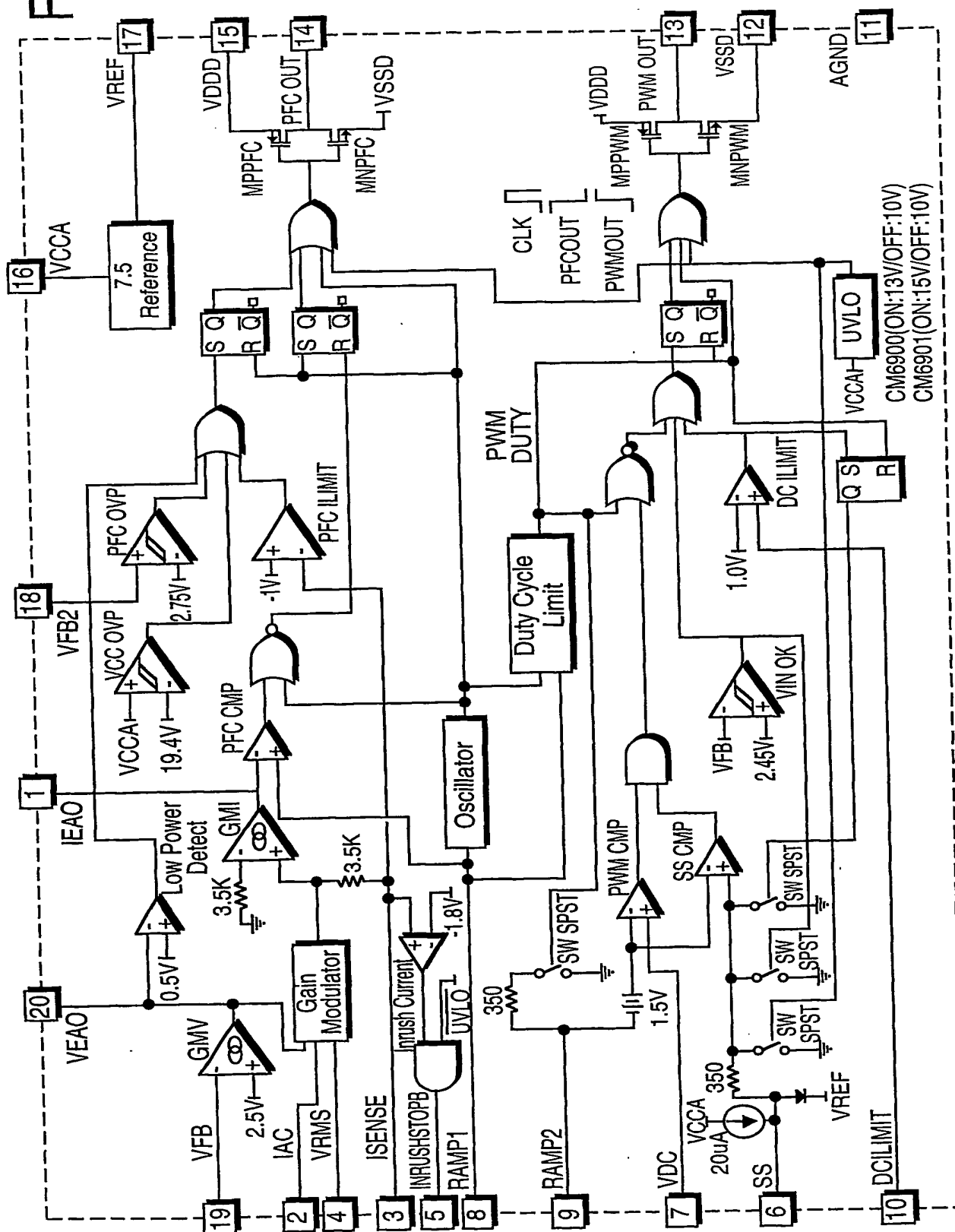


FIG. 4

FIG. 5A



SUBSTITUTE SHEET (RULE 26)

7/9

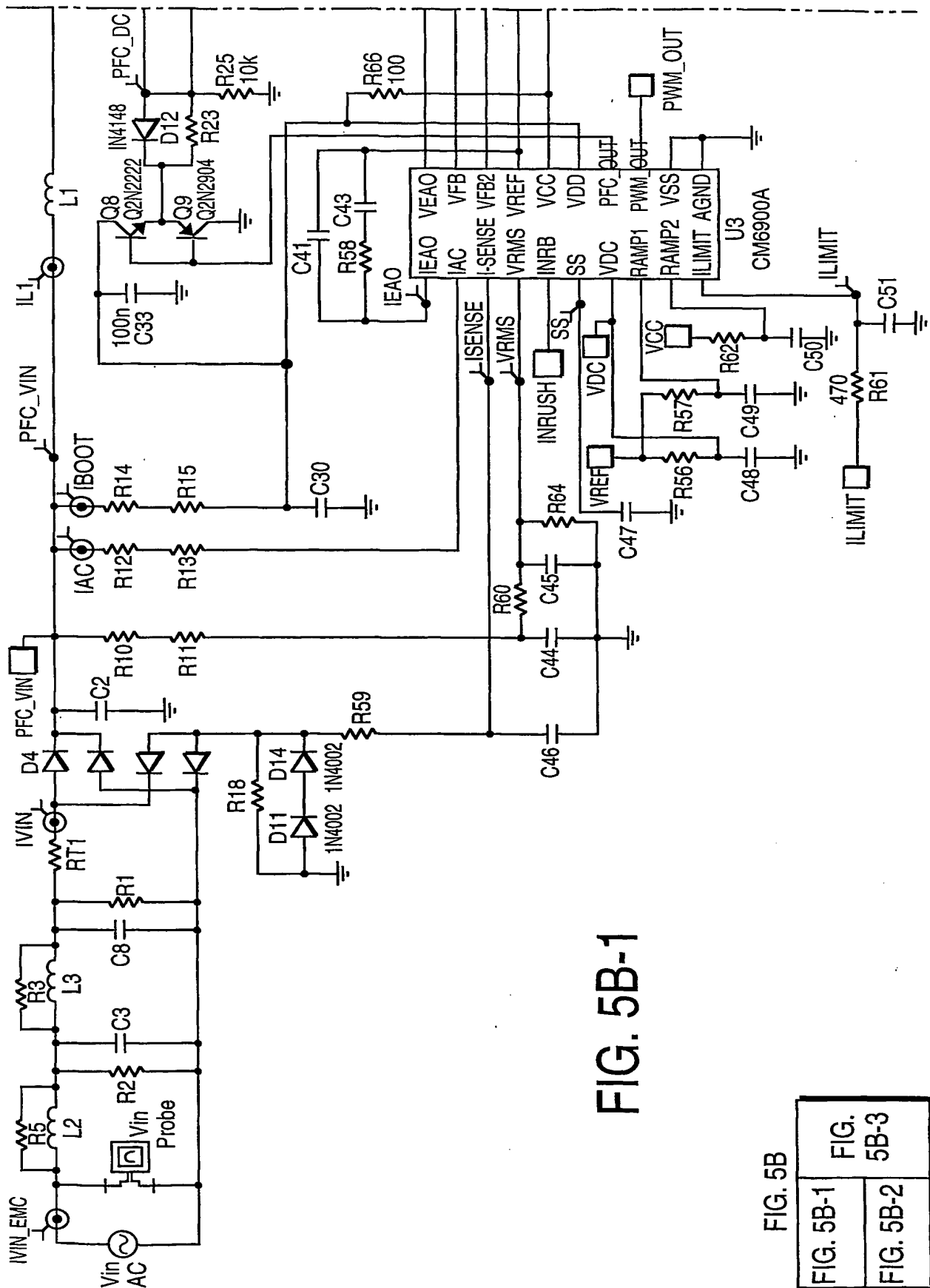


FIG. 5B-1

FIG. 5B

FIG. 5B-1	FIG. 5B-3
FIG. 5B-2	

8/9

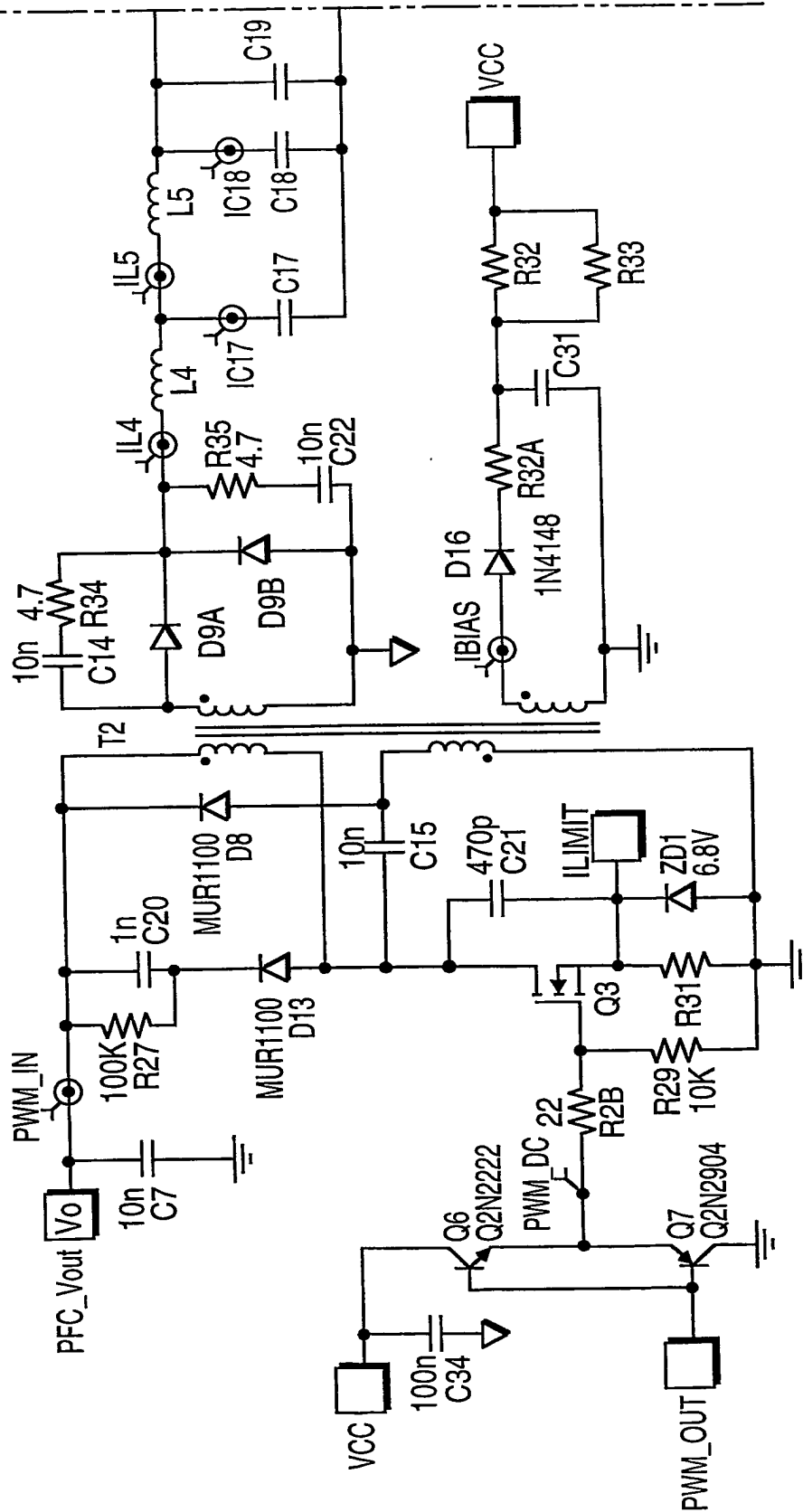


FIG. 5B-2

SUBSTITUTE SHEET (RULE 26)

9/9

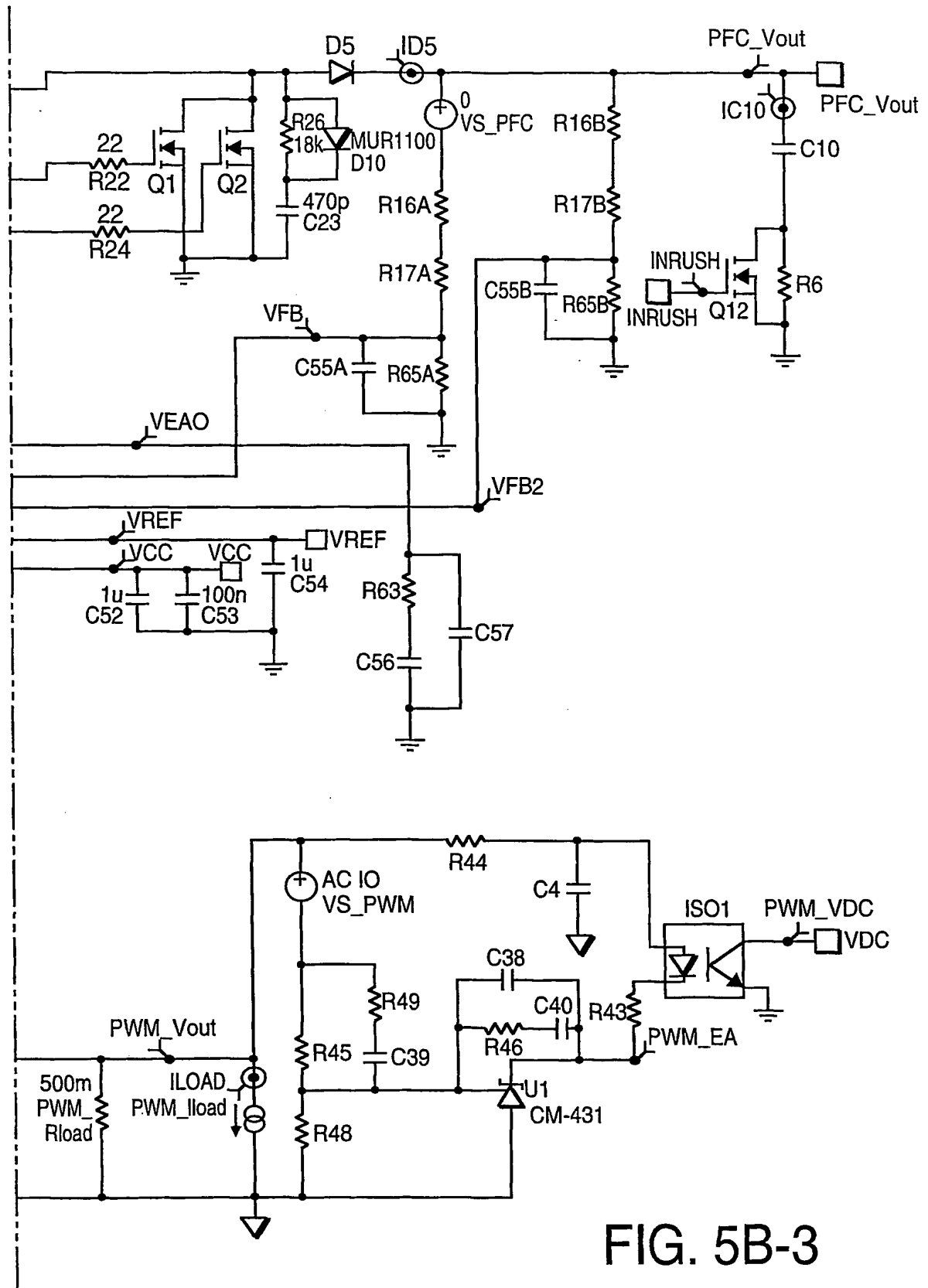


FIG. 5B-3

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US02/19890

A. CLASSIFICATION OF SUBJECT MATTER

IPC(7) : G05F 1/46, 1/56, 1/565, 1/573

US CL : 323/282, 283, 284, 351

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 323/282, 283, 284, 351

Documentation searched other than minimum documentation to the extent that such documents are included in the fields
searchedElectronic data base consulted during the international search (name of data base and, where practicable, search terms used)
NONE

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 4,754,388 A (POSPISIL) 28 June 1988 (28.06.1988), col. 4, line 46 to col.5, line 25.	1-27
X	US 5,859,527 A (COOK) 12 January 1999 (12.01.1999), see entire document.	1-27
A,P	US 6,346,778 B1 (MASON et al.) 12 February 2002 (12.02.2002), see entire document.	1, 13 and 17

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

"A"	document defining the general state of the art which is not considered to be of particular relevance	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"E"	earlier document published on or after the international filing date	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"O"	document referring to an oral disclosure, use, exhibition or other means	"Z"	document member of the same patent family
"P"	document published prior to the international filing date but later than the priority date claimed		

Date of the actual completion of the international search

29 AUGUST 2002

Date of mailing of the international search report

30 SEP 2002

Name and mailing address of the ISA/US
Commissioner of Patents and Trademarks
Box PCT
Washington, D.C. 20231

Facsimile No. (703) 305-3230

Authorized officer

ADOLF BERHANE

Telephone No. (703) 308-3299

Form PCT/ISA/210 (second sheet) (July 1998)*